

Description

The VPE2508 is a frequency adjustable, 1.5A, current-mode step-down converter with an integrated high-side switch. The VPE2508 operates with the wide input voltage from 4.5V to 60V and provides an adjustable output voltage from 0.8V to 48V.

The VPE2508 features a PWM mode operation with up to 1.5MHz adjustable switching frequency. The VPE2508 also provides a highly efficient solution with current mode control for fast loop response and easy compensation. The VPE2508 automatically enters PSM mode at light load.

Cycle-by-cycle current limiting and thermal shutdown are provided for fault condition protections. An internal 2ms soft-start design reduces input start-up current and prevents the output voltage and inductor current from overshooting during power-up.

The VPE2508 is available in E-SOP-8L with thermally enhanced package.

Typical Application

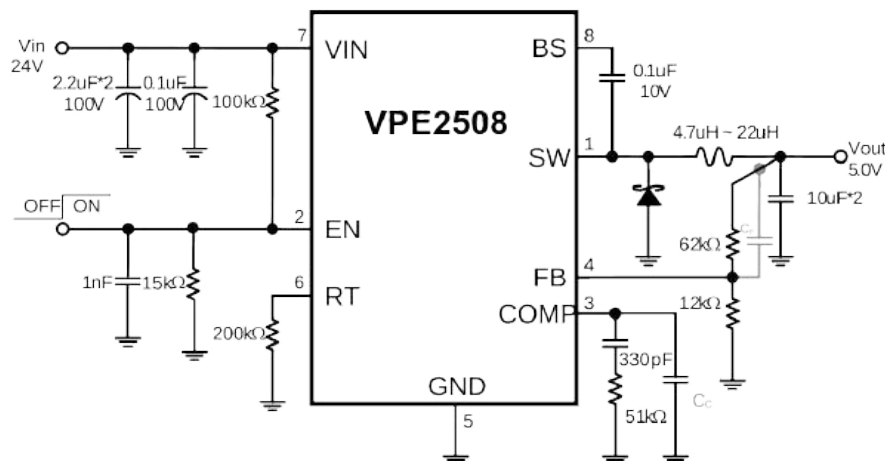
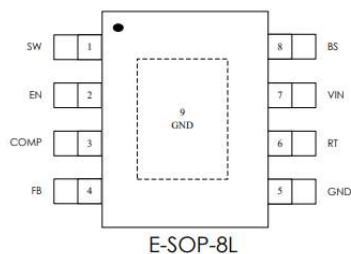


Figure. 1 VPE2508 application circuit

Package Configuration



VPE2508-00SG08NRR

00 Adjustable Output

SG08 E-SOP-8L Package

NRR RoHS & Halogen free package

Commercial Grade Temperature

Rating: -40 to 85°C

Package in Tape & Reel

Order, Mark & Packing information

Package	Vout(V)	Product ID	Marking Code	Packing
E-SOP-8L	Adjustable	VPE2508-00SG08NRR	2508	Tape & Reel 3K units

Pin Functions

Name	E-SOP-8L	Function
SW	1	Switch Out. This is the output from the high-side switch.
EN	2	Enable Pin. On/Off control Input. A 100k Ω pull-up resistor is recommended.
COMP	3	Compensation. This node is the output of Error Amplifier. Control loop frequency compensation is applied to this pin.
FB	4	Feedback Pin. This pin can be connected a resistor divider to set the output voltage range.
GND	5	Ground Pin. Connect exposed pad to GND plane for optimal thermal performance.
RT	6	Frequency setting pin. This pin can be connected to a resistor to GND to set the oscillator frequency (200kHz~1.5MHz adjustable switching frequency).
VIN	7	Supply Voltage. The VPE2508 operates from a 4.5V to 60V.
BS	8	Bootstrap. This is the positive power supply for the internal floating high-side MOSFET driver. Connect a bypass capacitor (0.1 μ F) between BS and SW.
GND	9	Ground Pin/Thermal Pad. This pin must be connected to ground. The thermal pad with large thermal land area on the PCB will be helpful for chip power dissipation.

Functional Block Diagram

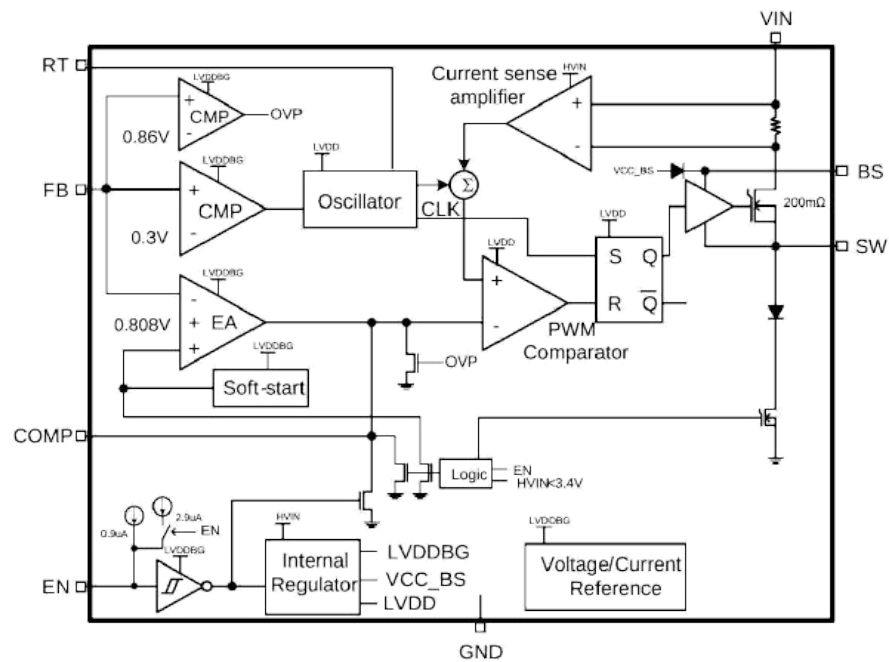


Fig. 2 Functional Block Diagram

Absolute Maximum Ratings

Devices are subjected to fail if they stay above absolute maximum ratings.

Input Voltage (V_{IN})	-0.3V to +66V	Lead Temperature (Soldering, 10 sec)	 260°C
Switch Voltage (SW)	-0.3V to $V_{IN}+0.3V$	Junction Temperature (Note 1)	-40°C to 150°C
Switch Voltage (SW, 10ns transient)	-1.6V to $V_{IN}+0.3V$	Storage Temperature Range	-65°C to 150°C
Bootstrap Voltage (BS)	 $V_{SW}-0.3V$ to $V_{SW}+6V$	ESD Susceptibility HBM	2KV
Enable Voltage (EN)	-0.3V to V_{IN}	MM	 200V
All Other Pins (RT, FB, COMP)	-0.3V to +6V		

Recommended Operating Conditions

Input Voltage (V_{IN})	+4.5V to +60V	Junction Operating Temperature Range	.. -40°C to 125°C
Ambient Operating Temperature Range	... -40°C to 85°C		

Thermal data

Package	Thermal Resistance	Parameter	Value
E-SOP-8L	θ_{JA} (Note 2)	Junction-ambient	50°C/W
	$\theta_{JC(top)}$ (Note 3)	Junction-case (top)	39°C/W
	$\theta_{JC(bottom)}$ (Note 4)	Junction-case (bottom)	10°C/W

Electrical Characteristics

$V_{IN}=12V$, $T_A=+25^{\circ}C$, unless otherwise specified.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Feedback Voltage	V_{FB}	$4.5V \leq V_{IN} \leq 60V$	0.788	0.808	0.828	V
Switch on Resistance	$R_{DS(ON)}$	-	-	200	300	m Ω
High-Side Switch Leakage	I_{SW}	$V_{EN}=0V$, $V_{SW}=0V$	-	-	10	μA
Current Limit	I_{LIM}	$F_{OSC}=500KHz$	2	2.5	-	A
COMP to Current Sensing Transconductance(Note 5)	G_{CS}	-	-	6.7	-	A/V
Error Amplifier Voltage Gain(Note 5)	A_{EA}	-	-	200	-	V/V
Error Amplifier Transconductance(Note 5)	G_{EA}	$I_{COMP}=\pm 3\mu A$	-	68	-	$\mu A/V$
Error Amplifier Min Source Current	-	$FB=0.7V$	-	5	-	μA
Error Amplifier Min Sink Current	-	$FB=0.9V$	-	-5	-	μA
V_{IN} UVLO Threshold	V_{UVLO}	-	3.9	4.2	4.5	V
V_{IN} UVLO Hysteresis	-	-	-	800	-	mV
Oscillation Frequency	F_{OSC}	$V_{FB}=0.6V$; $R_T=180k\Omega$	480	580	680	kHz
Fold-Back Frequency	-	$V_{FB}=0V$; $R_T=180k\Omega$	50	125	175	kHz
Shutdown Supply Current	I_{SD}	$V_{EN}=0$	-	10	20	μA
Quiescent Supply Current	I_Q	$V_{EN}=2V$, $V_{FB}=1V$, non-switching supply current	-	0.6	1.0	mA
Thermal Shutdown	T_{SD}	-	-	150	-	$^{\circ}C$
Thermal Shutdown Hysteresis	-	-	-	20	-	$^{\circ}C$
Minimum Off Time(Note 5)	T_{OFF}	-	-	200	-	ns
Minimum On Time(Note 5)	T_{ON}	-	-	150	-	ns
EN Input Low Voltage	-	-	-	-	0.4	V
EN Input High Voltage	-	-	1.5	-	-	V

- **Note 1:** T_J is a function of the ambient temperature T_A and power dissipation P_D ($T_J = T_A + (P_D \cdot \theta_{JA})$).
- **Note 2:** θ_{JA} is simulated in the natural convection at $T_A=25^{\circ}C$ on a highly effective thermal conductivity (thermal land area completed with $>3*3cm^2$ area) board (2 layers, 2S0P) according to the JEDEC 51-7 thermal measurement standard.
- **Note 3:** $\theta_{JC(top)}$ represents the heat resistance between the chip junction and the top surface of package.
- **Note 4:** $\theta_{JC(bottom)}$ represents the heat resistance between the chip junction and the center of the exposed pad on the underside of the package.
- **Note 5:** Guaranteed by design.

Typical Performance Characteristics

$V_{IN}=12V$, $V_{OUT}=5.0V$, $T_A=25^{\circ}C$, unless otherwise specified.

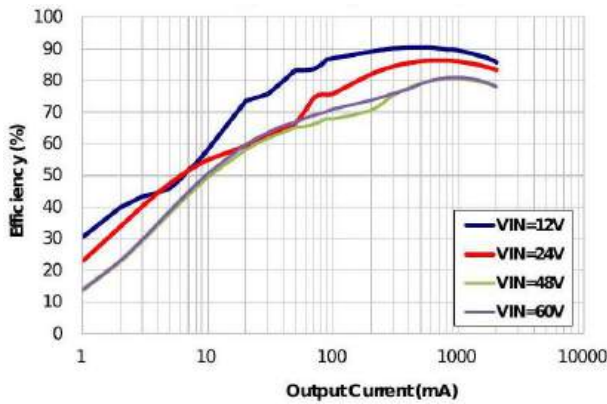


Figure 3. Efficiency vs. Output Current

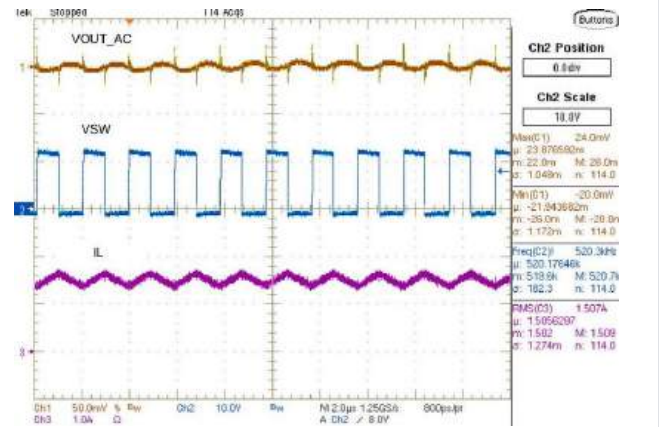


Figure 4. Output Ripple Voltage

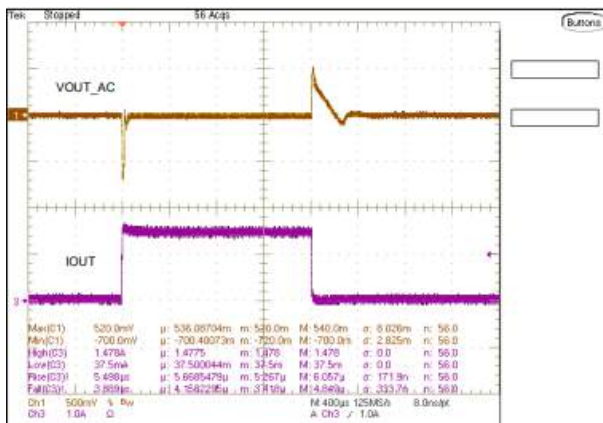


Figure 5. Load Transient (10mA→1.5A→10mA)

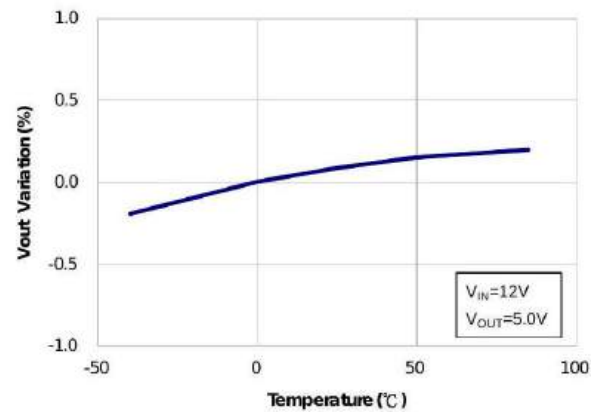


Figure 6. Output Voltage vs. Temperature

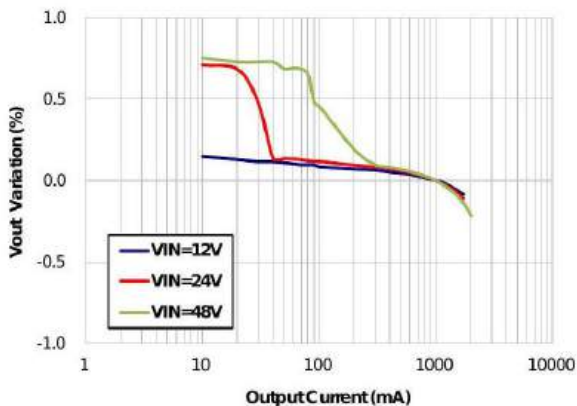


Figure 7. Load Regulation

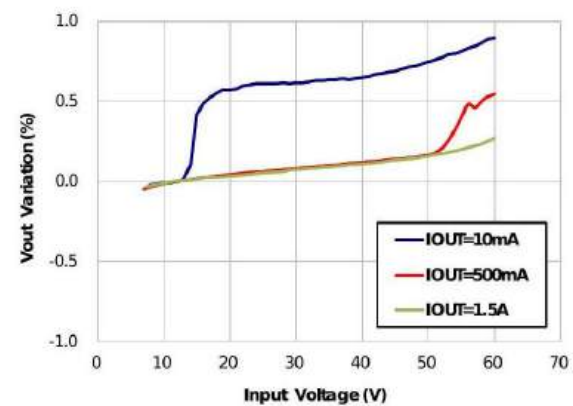


Figure 8. Line Regulation

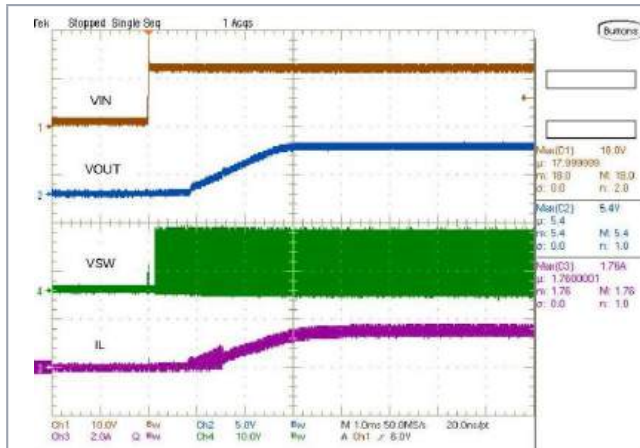


Figure 9. Power ON with 1.5A Load

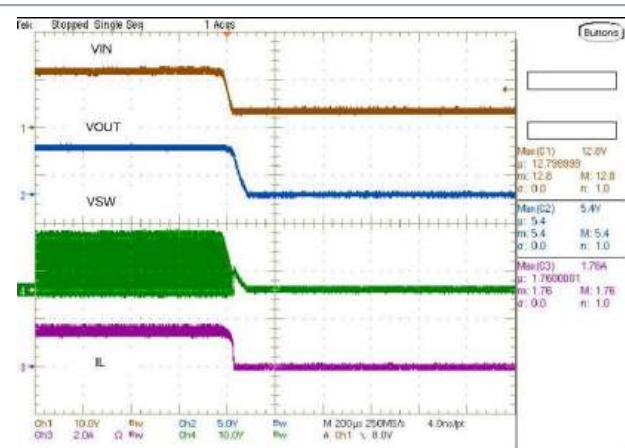


Figure 10. Power OFF with 1.5A Load

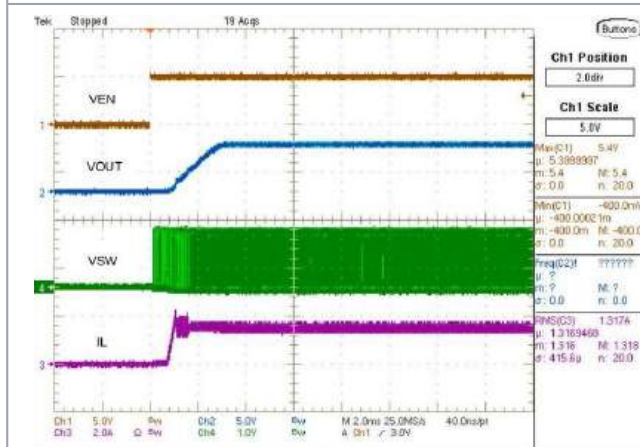


Figure 11. EN ON with 1.5A Load

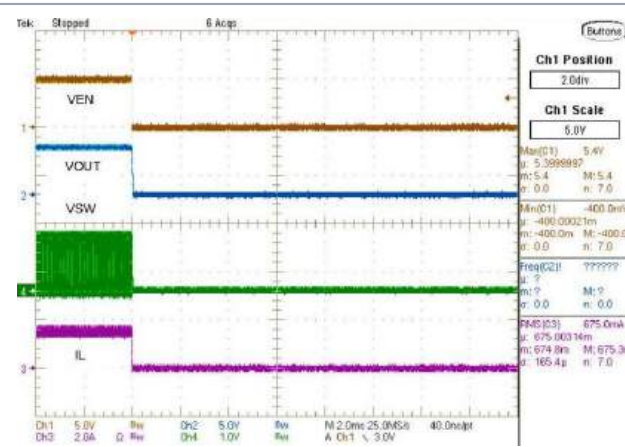


Figure 12. EN OFF with 1.5A Load

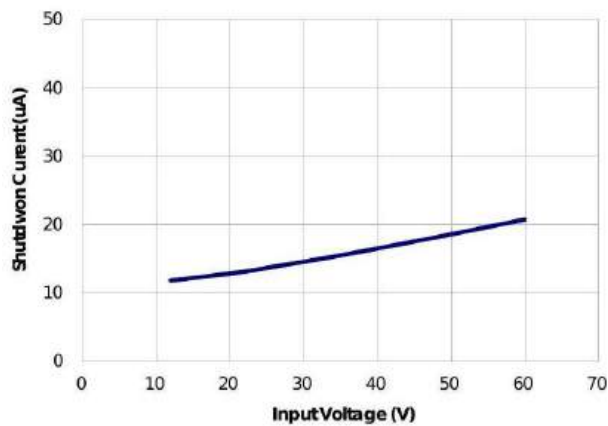


Figure 13. Shutdown Current vs. Input Voltage

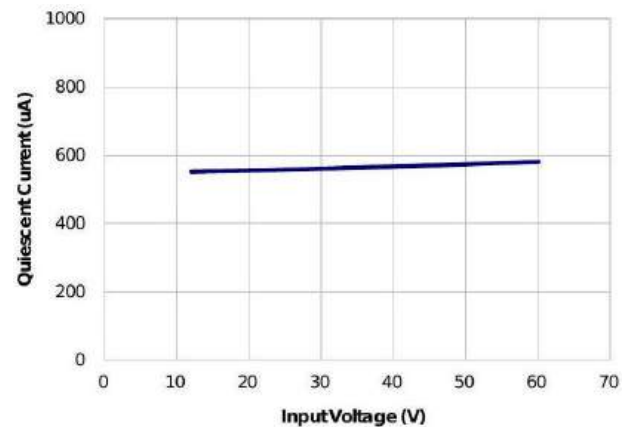


Figure 14. Quiescent Current vs. Input Voltage

Detailed Description

The VPE2508 is a variable frequency, current mode, buck converter with an integrated high-side switch. The device operates with input voltages from 4.5V to 60V and tolerates input transients up to 66V. During light-load conditions, the device enters Pulse Skip Mode, automatically.

Wide Input Voltage Range (4.5V to 60V)

The VPE2508 includes two separate supply inputs, VIN and BS, specified for a wide 4.5V to 60V input voltage range. VIN provides power to the device and BS provides power to the internal high-side switch driver. With respect to PWM minimum duty limit in VPE2508, the safe operating voltage area shall be considering in here. The Safe Operating Voltage Area (SOVA) is showed in the Fig.15.

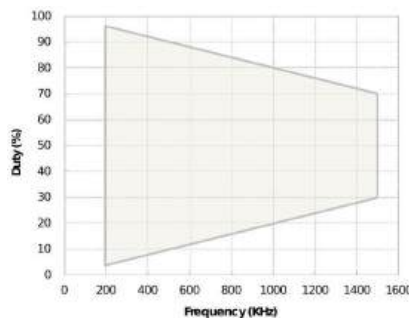


Fig. 15 VPE2508 Safe Operating Voltage Area

Error Amplifier

The error amplifier compares the FB pin voltage with the internal 0.8V reference and outputs a current proportional to the difference between the two. This output current is then used to charge or discharge the external compensation network on COMP pin to form the COMP voltage, which is used to control the power MOSFET current. During operation, the COMP voltage is range from 0.2V to 2.0V. COMP is internally pulled down to GND in shutdown mode. The voltage over 2.6V on COMP pin is not allowed due to 2.6V internal power.

Minimum On-Time

The device features a 150ns minimum on-time that ensures proper operation at high switching frequency and high differential voltage between the input and the output.

Enable Control

The VPE2508 has a dedicated enable control pin, EN. By pulling it high or low, that can be enabled and disabled. Tie EN to VIN through a 100kΩ resistor for automatic start up.

Over-Temperature Protection

Thermal overload protection limits the total power dissipation in the device. When the junction temperature exceeds 150°C, an internal thermal sensor shuts down the whole chip. The thermal sensor turns on the IC again after the junction temperature is cooled by 20°C.

Under Voltage Lock-out (UVLO)

UVLO is implemented to protect the chip from operating at insufficient supply voltage. The UVLO rising threshold is about 4.2V while its falling threshold is about 3.4V. If a higher UVLO is required for a specified application, as the EN pin had shown in Fig.16 below to adjust input voltage UVLO via two external resistors.

The EN enable threshold is around 1.0V (EN_{ON}), and with 100mV hysteresis window (EN_{OFF}) for shutdown. An internal pull-up current source I_E (1μA) is in default operating when EN pin floats. Once the EN pin voltage exceed the EN_{ON} , an additional 3μA of hysteresis, I_H , is added. This additional current facilitates adjustable input voltage UVLO hysteresis. Use Equation (a) to set the external UVLO hysteresis voltage. Use Equation (b) to set the external UVLO start voltage. For example, choosing $R_3=330k\Omega$ and $R_4=43k\Omega$, the external UVLO $V_{UVLO.start}$ and $V_{UVLO.stop}$ would be around 9V and 7V.

$$R_3 = \frac{V_{UVLO_start} - k V_{UVLO_stop}}{k 4\mu - 1\mu} \dots\dots\dots(a)$$

$$R_4 = \frac{EN_{on}}{\frac{V_{UVLO_start} - EN_{on}}{R_3} + 1\mu} \dots\dots\dots(b)$$

$$k = \frac{EN_{on}}{EN_{off}} = 1.1$$

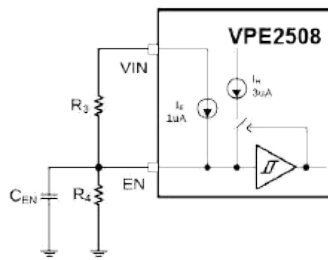


Fig. 16 External UVLO Lock-out

Bootstrap Capacitor

Connect a 0.1uF capacitor between the BS pin and SW pin. This capacitor provides the gate driver voltage for the high-side MOSFET. Also, an UVLO in the floating supply is implemented to protect the high-side MOSFET and its driver from operating at insufficient supply voltage. The UVLO rising threshold is about 2.2V while its hysteresis is about 0.16V.

Over-Current Protection

Over-current limiting is implemented by sensing the drain-to-source voltage across the high-side MOSFET. The drain to source voltage is then compared to a voltage level representing the over-current threshold limit. If the drain-to-source voltage exceeds the over-current threshold limit, the over-current indicator is set true. Once over-current indicator is set true, over-current limiting is triggered. The high-side MOSFET is turned off for the rest of the cycle. The output voltage will start to drop if the output is dead-short to ground, suddenly. Once the FB is lower than 0.3V, the switching frequency of VPE2508 is down to around quarter of setting frequency till the dead-short event is removed.

Over-Voltage Protection

The VPE2508 is with an output voltage protection circuit to minimize output voltage overshoot when fast unload transients or fast supply transients or recovering from overloaded conditions, especially in application design with high inductance and low output capacitance. If the FB pin voltage is rising over 108% of reference voltage ($V_{ref}=0.8V$), the high side MOS is turned-off immediately. When the FB pin voltage drops below 104% of reference voltage, the high side MOS goes to normal operation.

Although there is an output overvoltage protection, the overshooting voltage would still be seen in designs with improper inductance (L) and output capacitance (C_{out}) due to the energy stored in inductor transfer to output capacitor. For example with $V_O=5V$, the output protection voltage $V_{O,OVP}=5V*1.08=5.4V$, the output overshoot voltage $V_{overshoot}$ would be around 5.6V during a fast load transient current (i) from 1.5A to 1mA with $L=22\mu H$ and $C_{out}=22\mu F$. The value of output overshoot voltage $V_{overshoot}$ can be calculated from:

$$V_{overshoot} = \sqrt{\frac{L}{C_{out}} i^2 + V_{O,OVP}^2}$$

Programmable Oscillator

The VPE2508 oscillating frequency (200kHz~1.5MHz adjustable switching frequency) is set by an external resistor, R_T from the R_T pin to GND. The value of R_T can be calculated from:

$$\text{Frequency(kHz)} = \frac{5.56 \cdot 10^4}{R_T^{0.889} \text{ (k}\Omega\text{)}}$$

Application Information

The schematic on the front page shows a typical application circuit. The IC can provide up to 1.5A output current at a 5V output voltage. For proper thermal performances, the exposed pad of the device must be soldered down to the PCB.

Setting the Output Voltage

The output voltage is set by the resistive voltage divider from the output voltage to FB pin. The voltage divider divides the output voltage down to the feedback voltage by the ratio:

$$V_{FB} = V_{OUT} \frac{R_2}{R_1 + R_2}, V_{OUT} = V_{FB} \frac{R_1 + R_2}{R_2}$$

Table1. Resistor Selection for Common Output Voltages

V _{OUT}	R1 (kΩ)	R2 (kΩ)
1.8V	14.8 (1%)	11.8 (1%)
2.5V	25 (1%)	11.8 (1%)
3.3V	37 (1%)	11.8 (1%)
5.0V	62 (1%)	11.8 (1%)
12V	166 (1%)	11.8 (1%)

Selecting the Inductor

The common rule for determining the inductance to use is to allow the peak-to-peak ripple current in the inductor to be between 20% and 40% of the DC maximum load current, typical 30%. And also have sufficiently high saturation current rating and a DCR as low as possible. Generally, it is desirable to have lower inductance in switching power supplies, because it usually corresponding to faster transient response, smaller DCR and reduced size for more compact designs. But too low of an inductance results in higher ripple current such that over-current protection at full load could be falsely triggered. Also, the output ripple voltage and efficiency become worse with lower inductance. Under light load condition, like below 100mA, larger inductance is recommended for improved efficiency. The inductance and its peak current could be calculated by:

$$L = \frac{V_{OUT}}{f_S \Delta I_L} \left(1 - \frac{V_{OUT}}{V_{IN}} \right)$$

$$I_{LP} = I_{LOAD} + \frac{\Delta I_L}{2} = I_{LOAD} + \frac{V_{OUT}}{2 f_S L} \left(1 - \frac{V_{OUT}}{V_{IN}} \right)$$

Which f_S is the switching frequency; I_{LOAD} is the load current.

The gate driver with sufficient supply voltage for high-side MOSFET requirement, the inductor values $L > 2\mu H/V \cdot V_{out}$ is must followed up with.

Table2. Inductor Selection Guide

Model	I _{SAT} (A)	DCR (mΩ)	Manufacture
VCMT104T-220MN5	4.6	60.4 (typ.)	CYNTEC

Selecting the Diode

The diode connected between SW and GND is the path for the inductor current during the high-side MOSFET turns off. Choose the diode with minimum forward voltage drop and recovery time, like Schottky. And, the reverse voltage rating is greater than maximum input voltage and whose current rating is greater than the maximum load current.

Table3. Diode Selection Guide

Diode	Voltage/Current Rating	Manufacture
BX310F	100V, 3A	PANJIT

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current for step-down converter to maintain the DC input voltage. Use low ESR capacitor for the best performance. The high frequency impedance of the capacitor should be lower than the input source impedance for bypassing the high frequency switching current locally. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. To prevent excessive voltage ripple at input, the relationship between the input ripple and the capacitance could be estimated by:

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S C_{IN}} \frac{V_{OUT}}{V_{IN}} \left(1 - \frac{V_{OUT}}{V_{IN}} \right)$$

For 1.5A output applications, two 2.2μF ceramic capacitors are sufficient.

Selecting the Output Capacitor

The output capacitor (C_O) is required to maintain the DC output voltage, keeps the output ripple small, and ensures regulation loop stability. The lower ESR capacitors are preferred to keep lower output ripple. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S L} \left(1 - \frac{V_{OUT}}{V_{IN}} \right) \left(R_{ESR} + \frac{1}{8 f_S C_O} \right)$$

Which L is the inductance and R_{ESR} is the equivalent series resistance (ESR) of the output capacitor.

In case of lower ESR capacitor adopted, the output ripple is mainly caused by the capacitance and the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 f_S^2 L C_O} \left(1 - \frac{V_{OUT}}{V_{IN}} \right)$$

Or, the ESR dominates the impedance at switching frequency. After simplification, the output voltage ripple can approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S L} \left(1 - \frac{V_{OUT}}{V_{IN}} \right) R_{ESR}$$

The characteristics of the output capacitor also affect the loop stability of regulation system. Low ESR ceramic capacitors with X5R or X7R dielectrics are recommended.

Compensation Components

The VPE2508 employs current mode control for easy compensation and fast transient response. The system stability and transient response are controlled through the COMP pin. COMP pin is the output of the internal error amplifier. A series capacitor-resistor combination sets a pole-zero combination to control the characteristics of the control system. The DC gain of the voltage feedback loop is given by:

$$A_{VDC} = R_L G_{CS} A_{EA} \frac{V_{FB}}{V_O}$$

Where R_L is the load resistor value, G_{CS} is the current sensing transconductance and A_{EA} is the error amplifier gain. The system has two important poles. One is due to the compensation capacitor (C_{CMP}) and the output resistor (r_O) of error amplifier, and the other is due to the output capacitor (C_O) and the load resistor (R_L). These poles are located at:

$$f_{p1} = \frac{1}{2\pi C_{CMP} r_O} = \frac{G_{EA}}{2\pi C_{CMP} A_{VEA}}$$

$$f_{p2} = \frac{1}{2\pi C_O R_L}$$

Where, G_{EA} is the error amplifier transconductance.

The system has one important zero, due to the compensation capacitor (C_{CMP}) and the compensation resistor (R_{CMP}). The zero is located at:

$$f_{Z1} = \frac{1}{2\pi C_{CMP} R_{CMP}}$$

The system may have another important zero, if the output capacitor has a large capacitance with a high ESR value. The zero, due to the ESR and a capacitance of the output capacitor, is located at:

$$f_{ESR} = \frac{1}{2\pi C_O R_{ESR}}$$

In this case, a third pole set by the compensation capacitor (C_C) which is directly connected to COMP Pin between GND and the compensation resistor (R_{CMP}) is used to compensate the effect of the ESR zero(f_{ESR}) on the loop gain. This pole is located at:

$$f_{p3} = \frac{1}{2\pi C_C R_{CMP}}$$

To shape the converter transfer function for getting an adequate loop gain is the purpose of compensation design. The system open loop unity gain crossover frequency is important. Lower crossover frequencies result in slower line and load transient responses, while higher crossover frequencies could system unstable. A good compromise is to set the crossover frequency to below one-tenth of the switching frequency. To optimize the compensation components, the following procedure can be used:

1. Choose the compensation resistor (R_{CMP}) to set the desired crossover frequency. Determine the R_{CMP} value by the following equation:

$$R_{CMP} = \frac{2\pi C_O f_C}{G_{EA} G_{CS}} \frac{V_O}{V_{FB}}$$

Where, f_C is the desired crossover frequency.

2. Choose the compensation capacitor (C_{CMP}) to get the desired phase margin. For applications with typical inductor values, setting the compensation zero, f_{Z1} , to below one-fourth of the crossover frequency provides sufficient phase margin. Determine the C_{CMP} value by the following equation:

$$C_{CMP} > \frac{4}{2\pi R_{CMP} f_C}$$

Where, R_{CMP} is the compensation resistor value. To avoid the output voltage unstable due to the parasitic capacitor between the COMP pin and GND, the $C_{CMP} > 100\text{pF}$ is strongly recommended.

3. Determine if the second compensation capacitor (C_C) is required. It is required if the ESR zero of the output capacitor is located at less than half of the switching frequency, the following relationship is valid:

$$\frac{1}{2\pi C_O R_{ESR}} < \frac{f_S}{2}$$

If this is the case, then add the second compensation capacitor C_C to set the pole f_{p3} at the location of the ESR zero. Determine the C_C value in the following equation:

$$C_C > \frac{C_O R_{ESR}}{R_{CMP}}$$

Table4. Components Selection Guide

V_{OUT} (V)	L (μH)	C_O (μF)	R_{CMP} (k Ω)	C_{CMP} (pF)	C_C (pF)
5	4.7~22	20	51	330	100

4. The estimation is based on 15% of I_{out} current for this table. User can calculate it depend on peak-to-peak ripple current real requirement.

External Bootstrap Diode

An external bootstrap diode is recommended to add between external 5V and BS pin to enhance efficiency of the regulator. The external 5V can be a 5V fixed input from system or a 5V output of the VPE2508. The low cost diode, like 1N4148, is sufficient. With such diode, 5V input voltage can output 3.3V and 2.5V with just 30mA load.

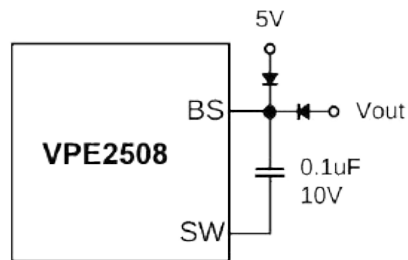
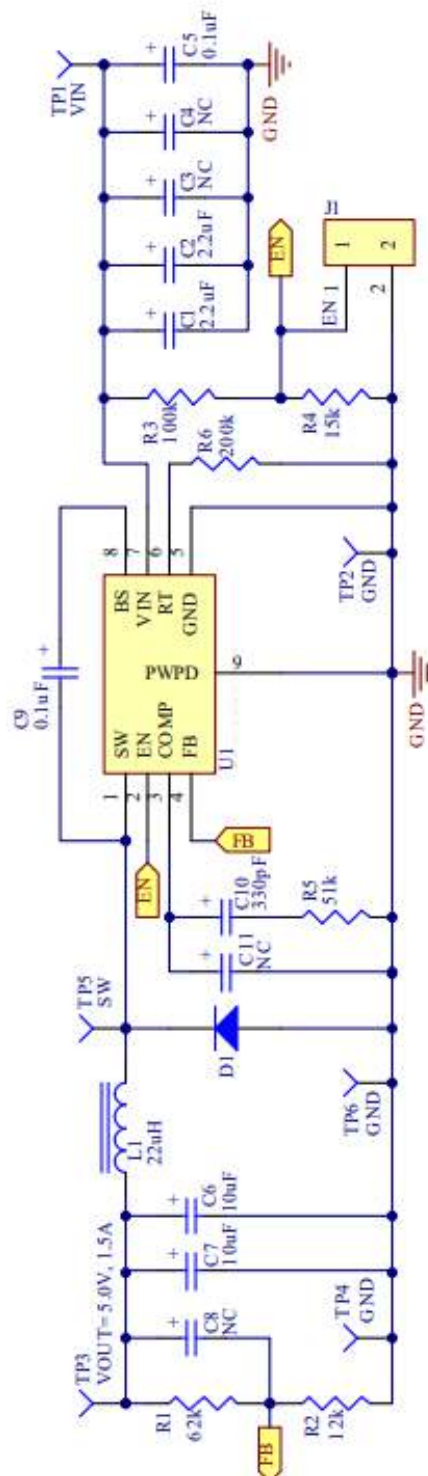


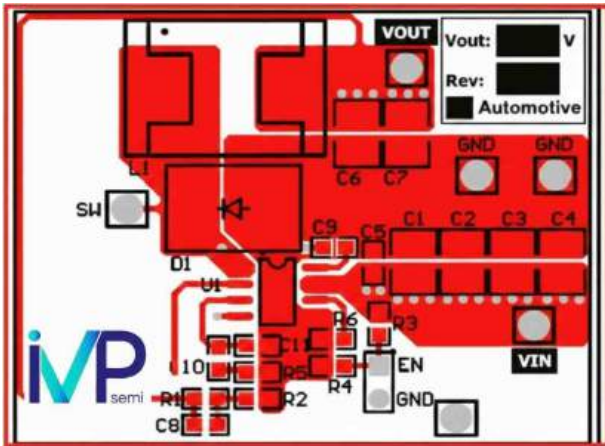
Fig. 17 External Bootstrap Diode

Applications

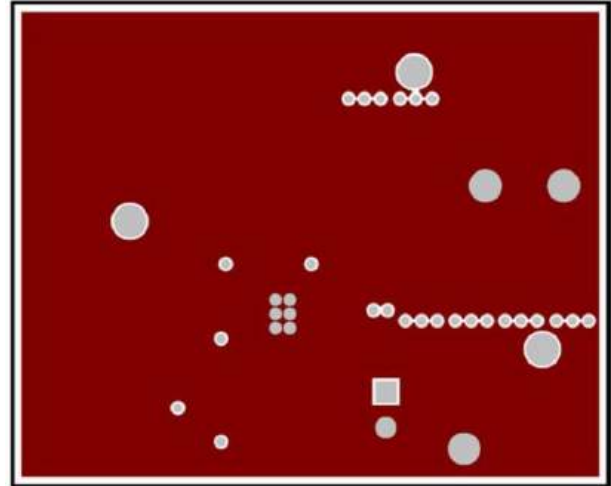
Typical schematic for PCB layout



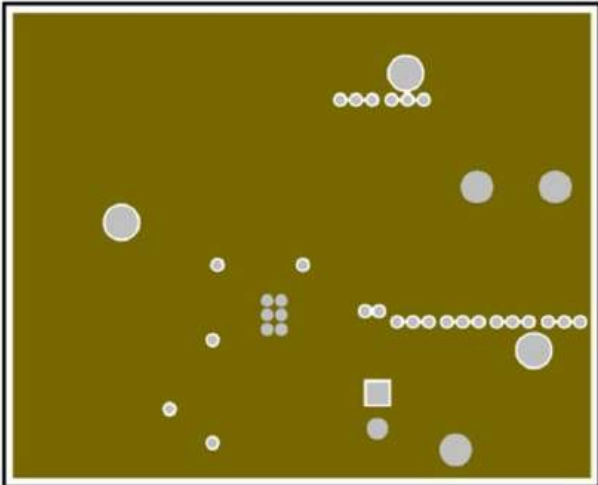
Typical schematic for PCB layout (cont.)



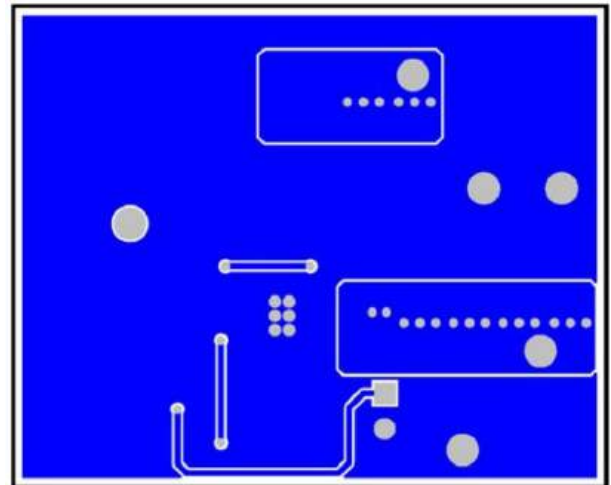
Top-Side Layout (Fig.18)



Layer 2 Layout (Fig.19)

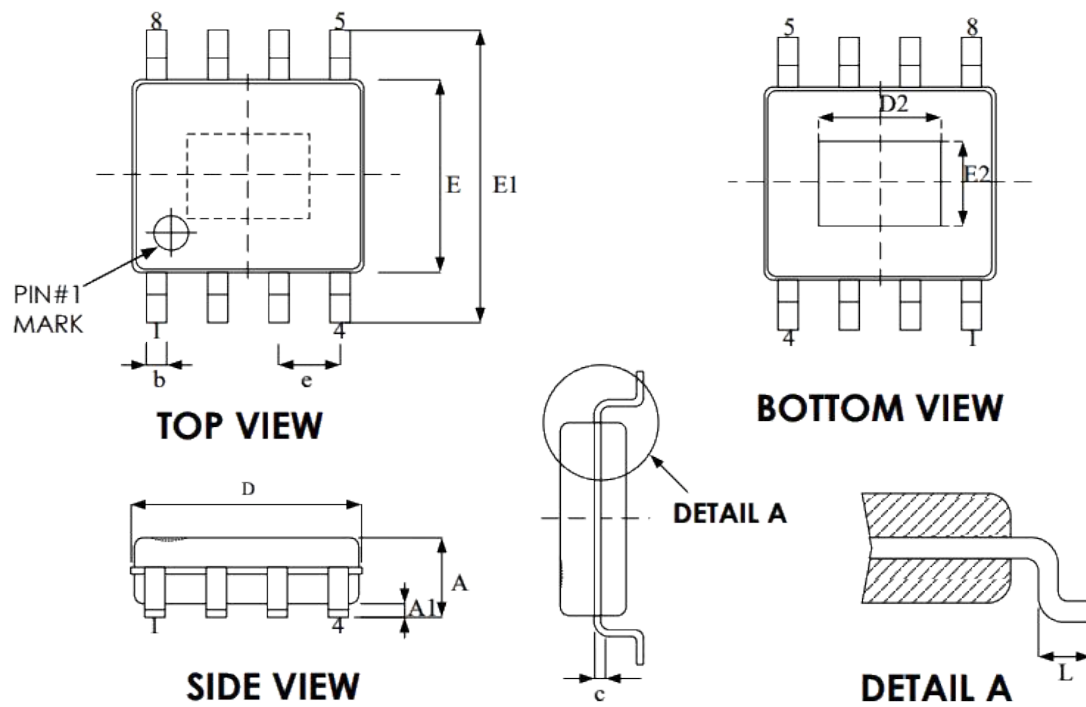


Layer 3 Layout (Fig.20)



Bottom-Side Layout (Fig.21)

Package Outline Drawing



E-SOP-8L (150 mil)

Symbol	Dimension in mm	
	Min.	Max.
A	-	1.70
A1	0.00	0.15
b	0.31	0.51
c	0.10	0.25
D	4.80	5.00
E	3.81	4.00
E1	5.79	6.20
e	1.27 BSC	
L	0.40	1.27

Exposed pad

Symbol	Dimension in mm	
	Min.	Max.
D2	2.80	3.50
E2	2.00	2.60

Disclaimer

The information provided in this datasheet is believed to be accurate and reliable. Errors or omissions are expected. indiaVP Semiconductor Pvt. Ltd. reserves the right to make changes to the product specifications without prior notice. Users should verify the suitability of the product for their specific applications. Please visit our website for the latest datasheet.

Contact Information

indiaVP Semiconductor Pvt. Ltd.

Email: sales@ivpsemi.com

Website: www.ivpsemi.com