VPE2507

Dual Channel 1MHz, 2A Synchronous Step-Down Regulator

Description

VPE2507 is a high efficiency step down DC/DC converter and supports dual channel for portable devices applications. It features an extremely low quiescent current, which is suitable for reducing standby power consumption, especially for portable applications.

The device can accept input voltage from 2.6V to 5.5V and deliver up to 2A output current. High 1MHz switching frequency allows the use of small surface mount inductors and capacitors to reduce overall PCB board space. Furthermore, the built-in synchronous switch improves efficiency and eliminates external Schottky diode. VPE2507 uses different modulation modes for various loading conditions: (1) Pulse Width Modulation (PWM) for low output voltage ripple and fixed frequency noise, (2) Pulse Frequency Modulation (PSM) for improving light load efficiency. In addition VPE2507 also builds in short circuit and over voltage protection.

The adjustable version of this device is available in TDFN-10L package.

Key Features

- Achieve 95% efficiency
- Input voltage: 2.6V to 5.5V
- Output current up to 2A
- Reference voltage: 0.6V
- Quiescent current 45μA
- Internal switching frequency: 1MHz
- No Schottky diode needed
- Low dropout operation: 100% duty cycle
- Shutdown current $< 1\mu A$
- Excellent line and load transient response
- Over-temperature protection
- Over Voltage protection
- Hiccup mode Short circuit protection

Applications

- Blue-Tooth devices
- Cellular and Smart Phones
- LCD TV Power Supply
- Wireless networking
- Portable applications

Typical Application

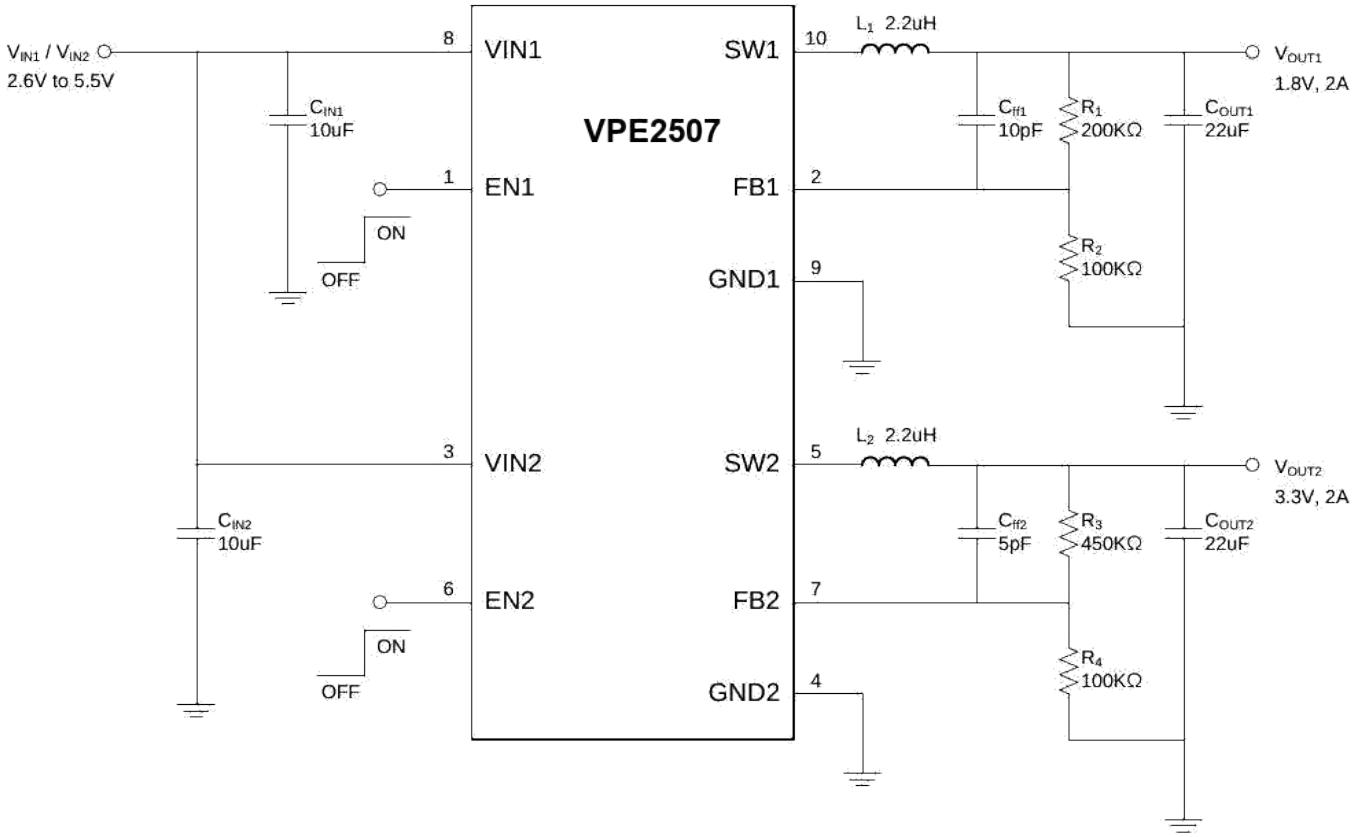
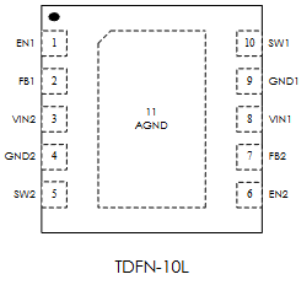


Figure 1. VPE2507 Typical Application Circuit

Package Configuration



TDFN-10L

TDFN-10L

VPE2507-XXFH10NRR

XX Output voltage

00 Adjustable

FH10 TDFN-10L Package

NRR RoHS & Halogen free package

Commercial Grade Temperature

Rating: -40 to 85℃

Package in Tape & Reel

Order, Mark & Packing information

Package	Vout(V)	Product ID	Marking Code	Packing
TDFN-10L	Adjustable	VPE2507-00FH10NRR	2507	Tape & Reel 5K units

Pin Functions

Name	TDFN-10L	Function
EN1	1	**Enable Pin1.** Minimum 1.5V to enable the device. Maximum 0.4V to shut down the device.
FB1	2	**Feedback Pin1.** Receives the feedback voltage from an external resistive divider across the output.
VIN2	3	**Power Input Pin2.** Must be closely decoupled to GND pin with a 10μF or greater ceramic capacitor.
GND2	4	**Ground Pin2.**
SW2	5	**Switch Pin2.** Must be connected to Inductor. This pin connects to the drains of the internal main and synchronous power MOSFET switches.
EN2	6	**Enable Pin2.** Minimum 1.5V to enable the device. Maximum 0.4V to shut down the device.
FB2	7	**Feedback Pin2.** Receives the feedback voltage from an external resistive divider across the output.
VIN1	8	**Power Input Pin1.** Must be closely decoupled to GND pin with a 10μF or greater ceramic capacitor.
GND1	9	**Ground Pin1.**
SW1	10	**Switch Pin1.** Must be connected to Inductor. This pin connects to the drains of the internal main and synchronous power MOSFET switches.
AGND	11	**Analog Ground Pin.**

Functional Block Diagram

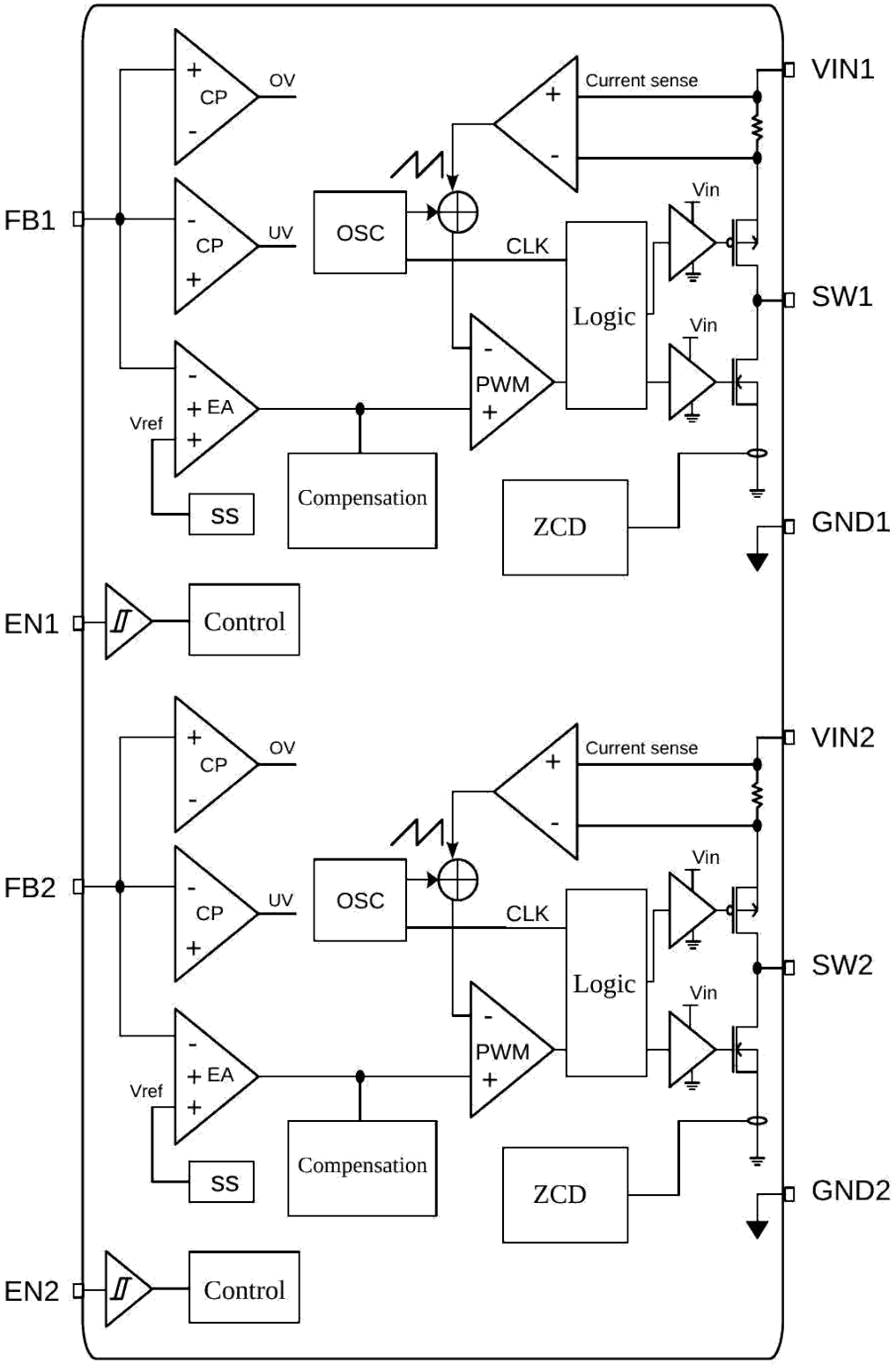


Figure 2. Functional Block Diagram of VPE2507

Absolute Maximum Ratings

Devices are subjected to fail if they stay above absolute maximum ratings.

Input Voltage ..... –0.3V to 6V
EN, FB Voltages ..... –0.3V to V_{IN}
SW Voltage ..... –0.3V to (V_{IN} + 0.3V)
Lead Temperature (Soldering, 10 sec) ..... 260°C

Operating Temperature Range ..... –40°C to 85°C
Junction Temperature (Notes 1, 3) ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
ESD Susceptibility HBM 2KV
ESD Susceptibility MM 200V

Recommended Operating Conditions

Input Voltage (V_{IN}) ..... +2.6V to +5.5V

Junction Operating Temperature ..... –40°C to 125°C

Thermal data

Package	Thermal Resistance	Parameter	Value
TDFN-10L (3mm×3mm)	θ_{JA} (Note 4)	Junction-ambient	110°C/W
	θ_{JT} (Note 5)	Junction-to-top of package	4.2°C/W

Electrical Characteristics

V_{IN}=3.6V, T_A=+25°C, unless otherwise specified.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Voltage Range	V_{IN}	-	2.6	-	5.5	V
Feedback Current	I_{VFB}	-	-	-	±100	nA
Regulated Feedback Voltage	V_{FB}	-	0.588	0.600	0.612	V
Peak Inductor Current	I_{PK}	V_{FB} = 0.5V	3.0	-	-	A
Quiescent Current	I_Q	V_{FB} = 0.65V	-	45	-	μA
Shutdown Current	I_{SD}	V_{EN} = 0V	-	0.1	-	μA
Oscillator Frequency	f_{OSC}	V_{FB} = 0.6V	-	1	-	MHz
$R_{DS(ON)}$ of PMOS	R_{ON}	I_{SW} = 100mA	-	90	-	mΩ
$R_{DS(ON)}$ of NMOS		I_{SW} = -100mA	-	60	-	mΩ
VIN UVLO Threshold	V_{UVLO}	-	-	2.2	2.4	V
VIN UVLO Hysteresis		-	-	150	-	mV
Maximum Duty cycle	D	-	100	-	-	%
Short circuit protection Threshold	V_{SCP}	V_{FB}	-	0.2	-	V
SW Leakage	I_{LSW}	V_{EN} = 0V, V_{SW} = 0V or 5V, V_{IN} = 5V	-	-	±1	μA
Enable Threshold	V_{EN}	-	1.5	-	-	V
Shutdown Threshold		-	-	-	0.4	V
EN Leakage Current	I_{EN}	-	-	-	±1	μA
Thermal Shutdown	T_{SD}	-	-	160	-	°C
Thermal Shutdown Hysteresis		-	-	30	-	°C
Soft start time	T_{SS}	-	-	1.0	-	mS

- **Note 1:** T_J is a function of the ambient temperature T_A and power dissipation P_D ($T_J = T_A + (P_D * 134.5°C/W)$).
- **Note 2:** Dynamic quiescent current is higher due to the gate charge being delivered at the switching frequency.
- **Note 3:** This IC has a built-in over-temperature protection to avoid damage from overloaded conditions.
- **Note 4:** θ_{JA} is measured in the natural convection at T_A=25°C on a highly effective thermal conductivity test board (2 layers, 2S0P) according to the JEDEC 51-7 thermal measurement standard.
- **Note 5:** θ_{JT} represents the heat resistance between the chip and the package top center.

Typical Performance Characteristics

V_{IN}=5.0V, T_A=25°C, unless otherwise specified.

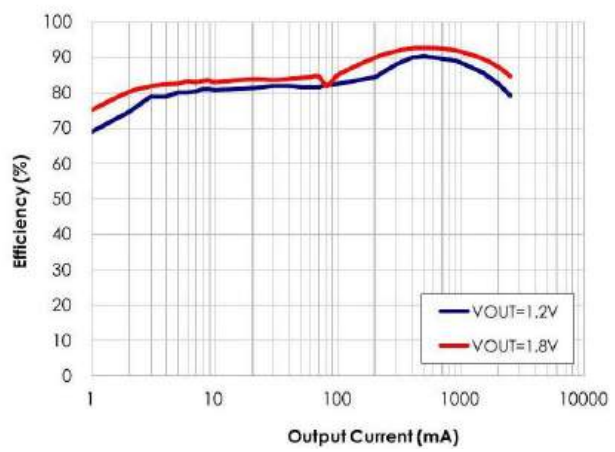


Figure 3. Efficiency vs. Output Current (V_{IN}=5V)

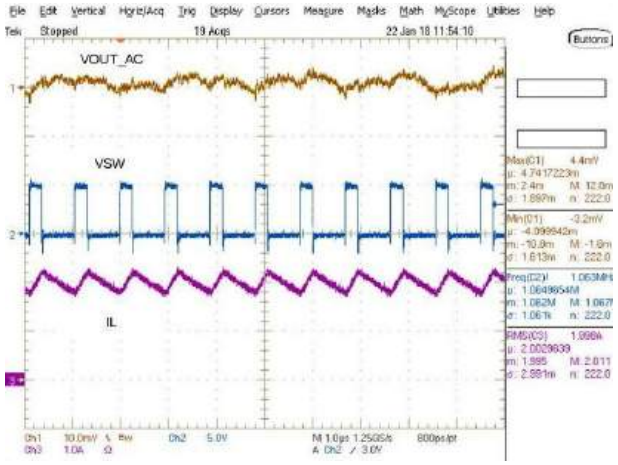


Figure 4. Output Ripple Voltage

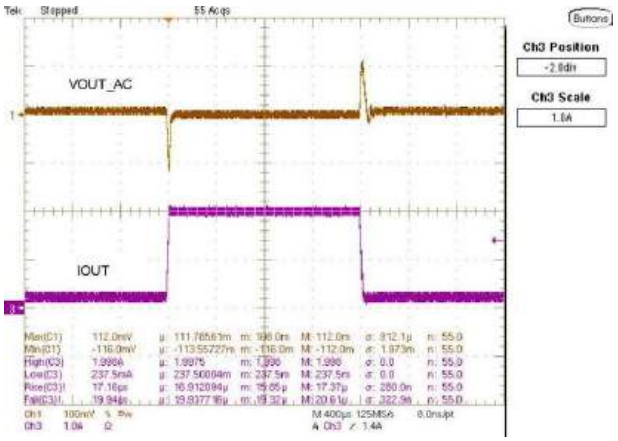


Figure 5. Load Transient (200mA→2A→200mA)

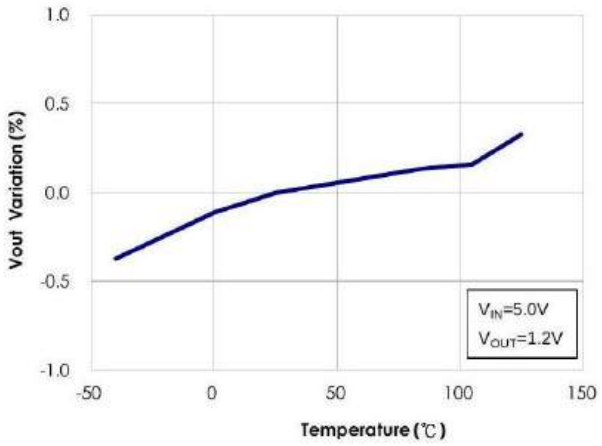


Figure 6. Vout Variation vs. Temperature

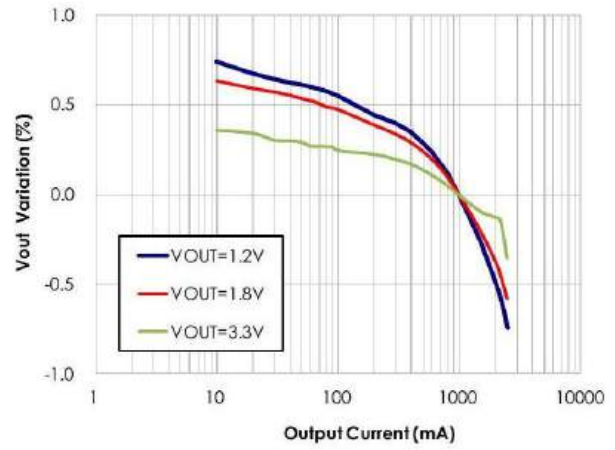


Figure 7. Load Regulation (V_{IN}=5V)

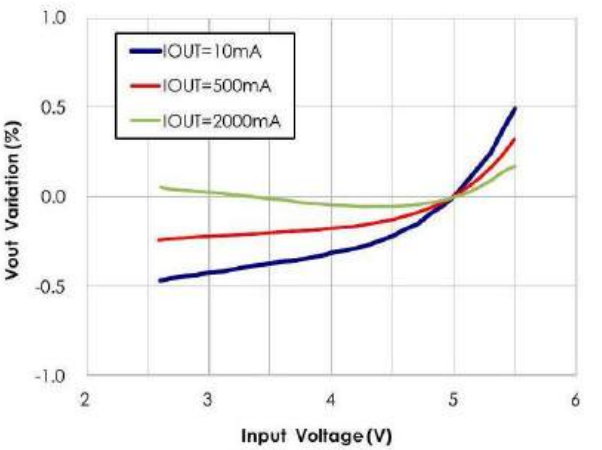


Figure 8. Line Regulation (V_{OUT}=1.2V)

Typical Performance Characteristics (Cont.)

V_{IN}=5.0V, T_A=25°C, unless otherwise specified.

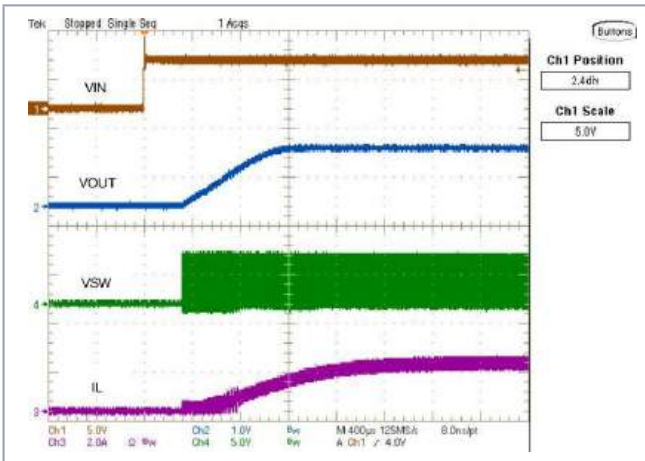


Figure 9. Power ON with 2A load

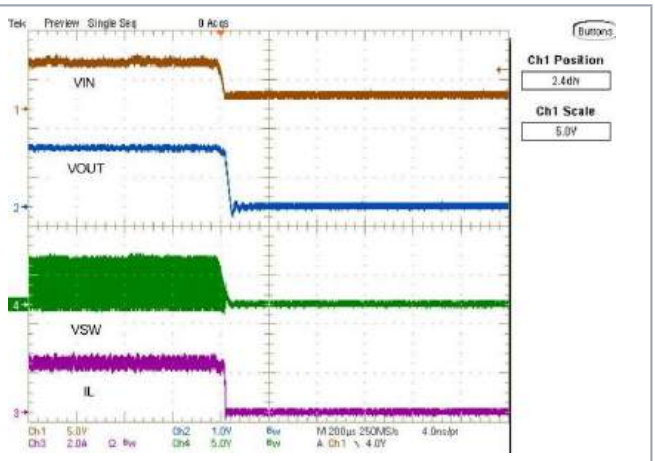


Figure 10. Power OFF with 2A load

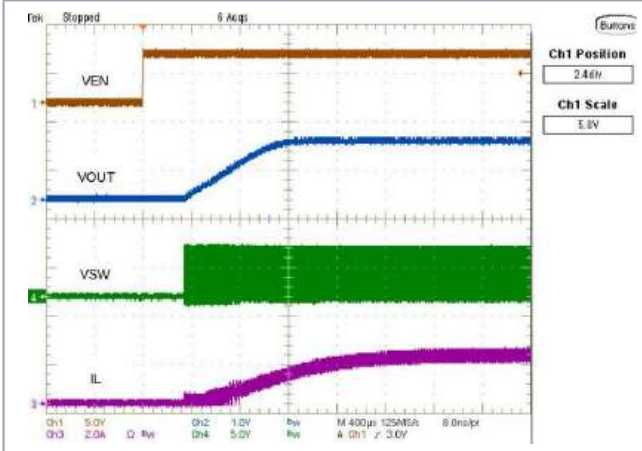


Figure 11. EN ON with 2A load

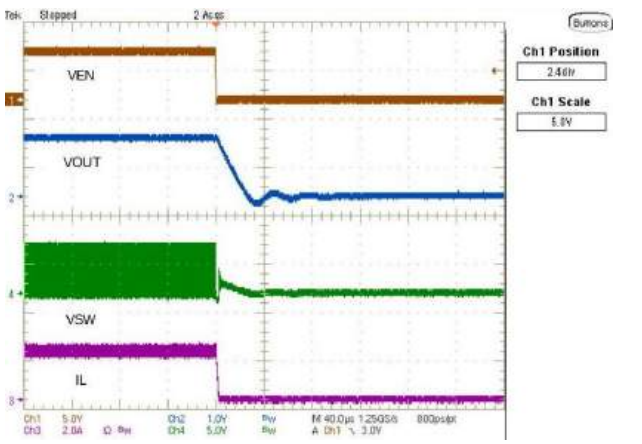


Figure 12. EN OFF with 2A load

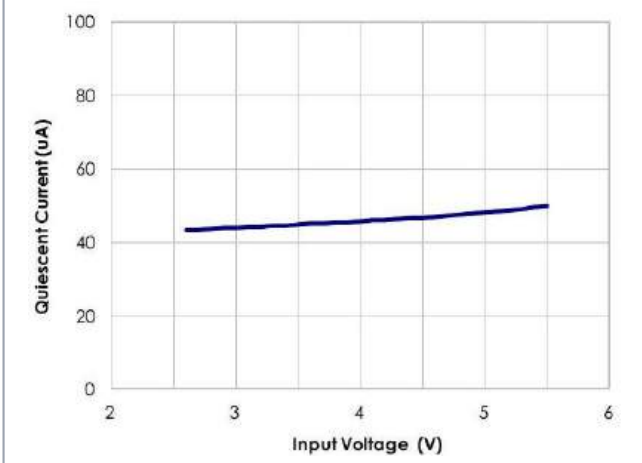


Figure 13. Quiescent Current vs. Input Voltage

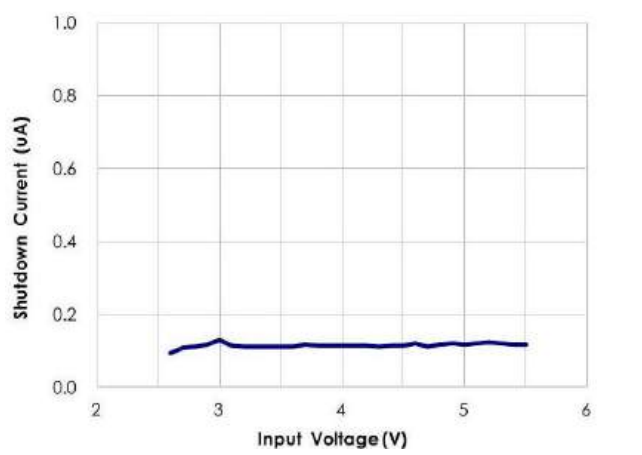


Figure 14. Shutdown Current vs. Input Voltage

Application Information

Inductor Selection

Inductor ripple current and core saturation current are the two main factors that decide the Inductor value. A low DCR inductor is preferred.

C_{IN} and C_{OUT} Selection

A low ESR input capacitor can prevent large voltage transients at V_{IN}. The RMS current of input capacitor is required larger than I_{RMS} calculated by:

$$I_{RMS} \cong I_{OMAX} \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}$$

ESR is an important parameter to select C_{OUT}, which can be seen in the following output ripple V_{OUT} equation:

$$\Delta V_{OUT} \cong \Delta I_L \left(ESR + \frac{1}{8 f C_{OUT}} \right)$$

Cheaper and smaller ceramic capacitors with higher capacitance values are now commercially available. These ceramic capacitors have low ripple currents, high voltage ratings and low ESR which make them suitable for switching regulator applications. It is feasible to optimize very low output ripples by C_{OUT} since C_{OUT} does not affect the internal control loop stability. X5R or X7R types are recommended since they have the best temperature and voltage characteristics of all ceramics capacitors.

Output Voltage (VPE2507 adjustable)

In the adjustable version, the output voltage can be determined by:

$$V_{OUT} = 0.6V \left(1 + \frac{R_1}{R_2} \right)$$

Some recommended value for common output voltage is listed below Table.1 :

Table.1- Recommended Component Selection

V_{OUT}(V)	R_1(KΩ)	R_2(KΩ)	C_{OUT}(μF)	C_{FF}(pF)	L(μH)
1.2	100	100	22*2	22	1.5
1.8	200	100	22	10	2.2
3.3	450	100	22	5	2.2

Thermal Considerations

Although the thermal shutdown circuit is designed in VPE2507 to protect the device from thermal damage, the total power dissipation that VPE2507 can sustain depends on the thermal capability of the package. The formula to ensure the safe operation is shown in note 1 on page 5. To avoid the VPE2507 from exceeding the maximum junction temperature, the user should perform some thermal analysis during PCB design.

PCB Layout Guidelines

To ensure proper operation of the VPE2507, please note the following PCB layout guidelines:

1. The GND, SW and the VIN trace should be kept short, direct and wide.
2. VFB pin must be connected directly to the feedback resistors. Resistive divider R_2/R_1 must be connected parallel to the output capacitor C_{OUT}.
3. The Input capacitor C_{IN} must be connected to the pin VIN as close as possible.
4. Keep SW node away from the sensitive VFB node since this node has high frequency and voltage swing.
5. Keep the (-) plates of C_{IN} and C_{OUT} as close as possible.

Applications

Typical schematic for PCB layout

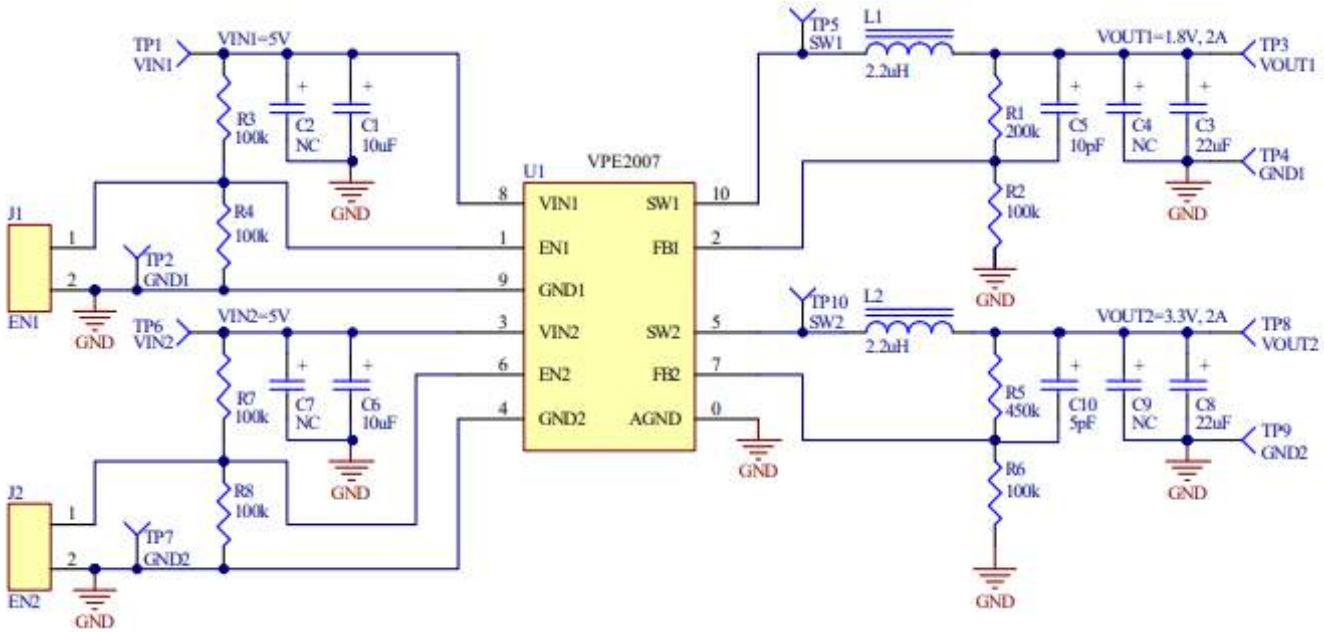


Figure 15. Typical Schematic of VPE2507

PCB Layout

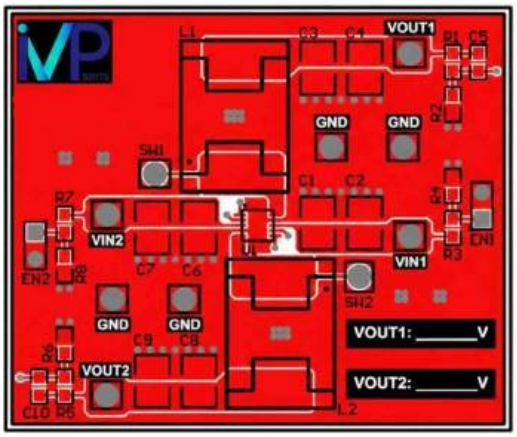


Figure 16. Top Layer

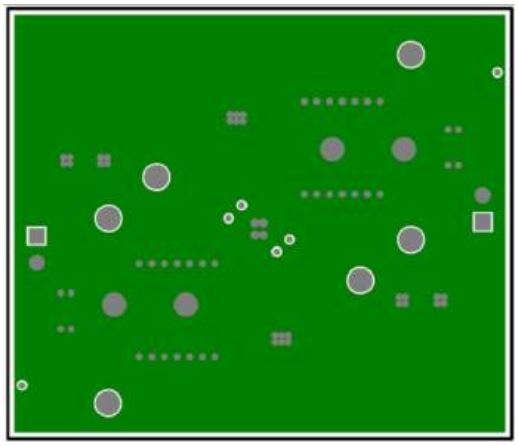


Figure 17. Mid1 Layer

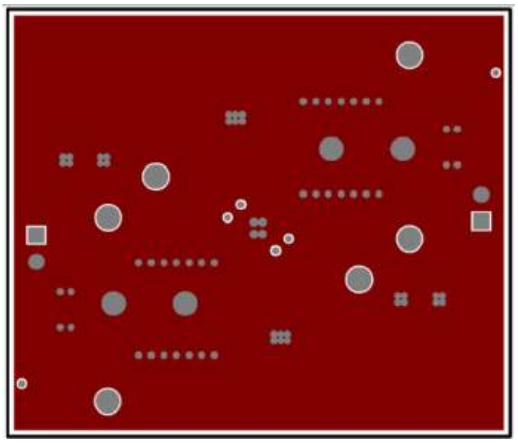


Figure 18. Mid2 Layer

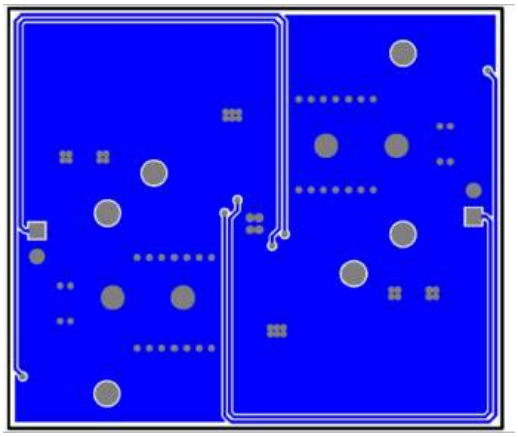
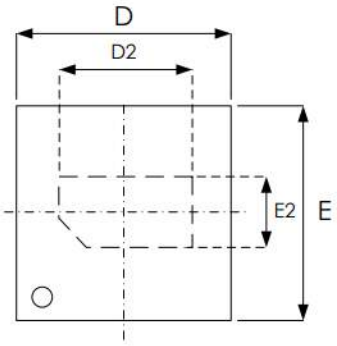
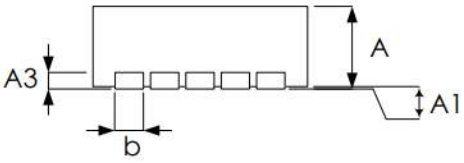


Figure 19. Bottom Layer

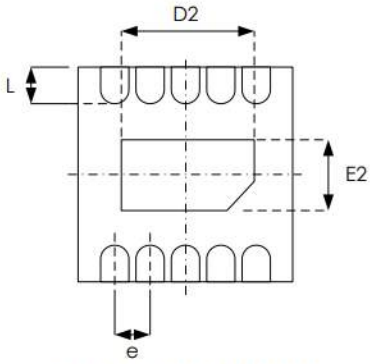
Package Outline Drawing (TDFN-10L (3mm×3mm))



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Symbol	Dimension in mm	
	Min.	Max.
A	0.70	0.85
A1	0.00	0.05
A3	0.18	0.25
b	0.18	0.30
D	2.90	3.10
E	2.90	3.10
e	0.5 BSC	
L	0.30	0.50

Exposed Pad

Symbol	Dimension in mm	
	Min.	Max.
D2	2.20	2.70
E2	1.40	1.75

Disclaimer

The information provided in this datasheet is believed to be accurate and reliable. Errors or omissions are expected. indiaVP Semiconductor Pvt. Ltd. reserves the right to make changes to the product specifications without prior notice. Users should verify the suitability of the product for their specific applications. Please visit our website for the latest datasheet.

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