VPE2503
3A, 36V, 2MHz Non-synchronous Step-Down Converter

Description

The VPE2503 is frequency adjustable, 3A, current-mode step-down converter with an integrated high-side switch. The VPE2503 operates with the wide input voltage from 4.5V to 36V and provides an adjustable output voltage from 0.808V to 30V. The VPE2503 features a PWM mode operation with up to 2MHz adjustable switching frequency.

The VPE2503 also provides a highly efficient solution with current mode control for fast loop response and easy compensation. The VPE2503 automatically enters PSM mode at light load.

Cycle-by-cycle current limiting and thermal shutdown are provided for fault condition protections. An internal 2ms soft-start design reduces input start-up current and prevents the output voltage and inductor current from overshooting during power-up.

The VPE2503 is available in E-SOP-8L and TDFN-10L with thermally enhanced package.

Key Features

- 4.5V to 36V Input Voltage Range
- 3A Continuous Output Current
- 120mΩ Internal Power MOSFET Switch
- Output Adjustable from 0.808V
- Output Over-Voltage Protection
- Up to 2MHz Adjustable Switching Frequency
- Cycle-by-Cycle Current Limit, Frequency Fold Back and thermal shutdown
- Stable with Low ESR Output Ceramic Capacitors
- 2ms Internal Soft-Start
- Thermally Enhanced E-SOP-8L Package

Applications

- 12V and 24V Distributed Power Systems
- Battery Powered Systems
- Industrial Power Systems
- LCD and Plasma TVs
- Automotive Systems

Typical Application

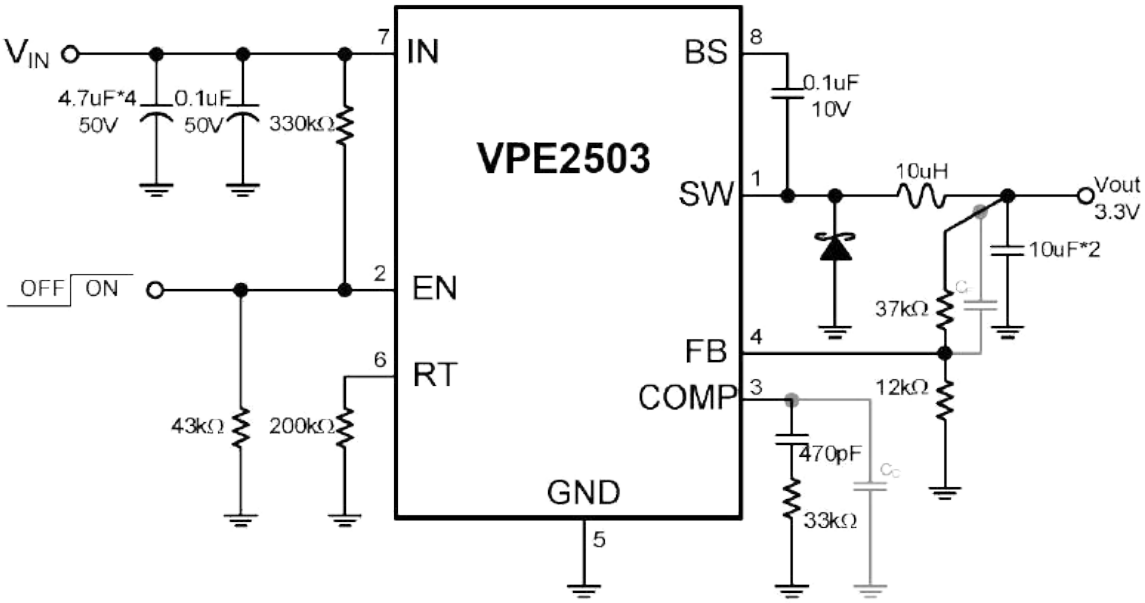
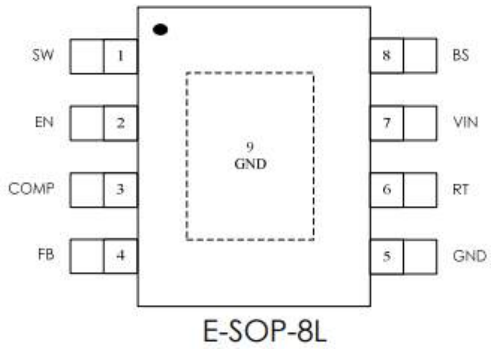


Figure 1. VPE2503 Typical Application Circuit

Package Configuration



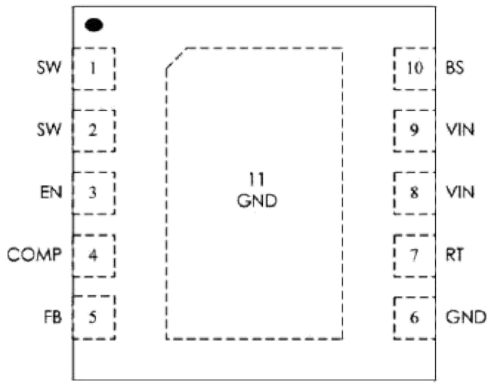
E-SOP-8L

VPE2503-00SG08NRR

00 Adjustable Output

SG08 E-SOP-8L Package

NRR RoHS & Halogen free package
Commercial Grade Temperature
Rating: -40 to 85℃
Package in Tape & Reel



TDFN-10L

VPE2503-00FH10NRR

00 Adjustable Output

FH10 TDFN-10L Package

NRR RoHS & Halogen free package
Commercial Grade Temperature
Rating: -40 to 85℃
Package in Tape & Reel

Order, Mark & Packing Information

Package	Vout(V)	Product ID	Marking Code	Packing
E-SOP-8L	Adjustable	VPE2503-00SG08NRR	2503	Tape & Reel 3K units
TDFN-10L	Adjustable	VPE2503-00FH10NRR	2503	Tape & Reel 5K units

Pin Functions

Name	E-SOP-8L	TDFN-10L	Function
SW	1	1,2	**Switch Out.** This is the output from the high-side switch.
EN	2	3	**Enable Pin.** On/Off control Input.
COMP	3	4	**Compensation.** This node is the output of Error Amplifier. Control loop frequency compensation is applied to this pin.
FB	4	5	**Feedback Pin.** This pin can be connected a resistor divider to set the output voltage range.
GND	5	6	**Ground Pin.** Connect exposed pad to GND plane for optimal thermal performance.
RT	6	7	**Frequency setting pin.** This pin can be connected to a resistor to GND to set the oscillator frequency.
VIN	7	8,9	**Supply Voltage.** The VPE2503 operates from a 4.5V to 36V.
BS	8	10	**Bootstrap.** This is the positive power supply for the internal floating high-side MOSFET driver. Connect a bypass capacitor (0.1uF) between BS and SW.
GND	9	11	**Ground Pin/Thermal Pad.** This Pin must be connected to ground. The thermal pad with large thermal land area on the PCB will helpful chip power dissipation.

Functional Block Diagram

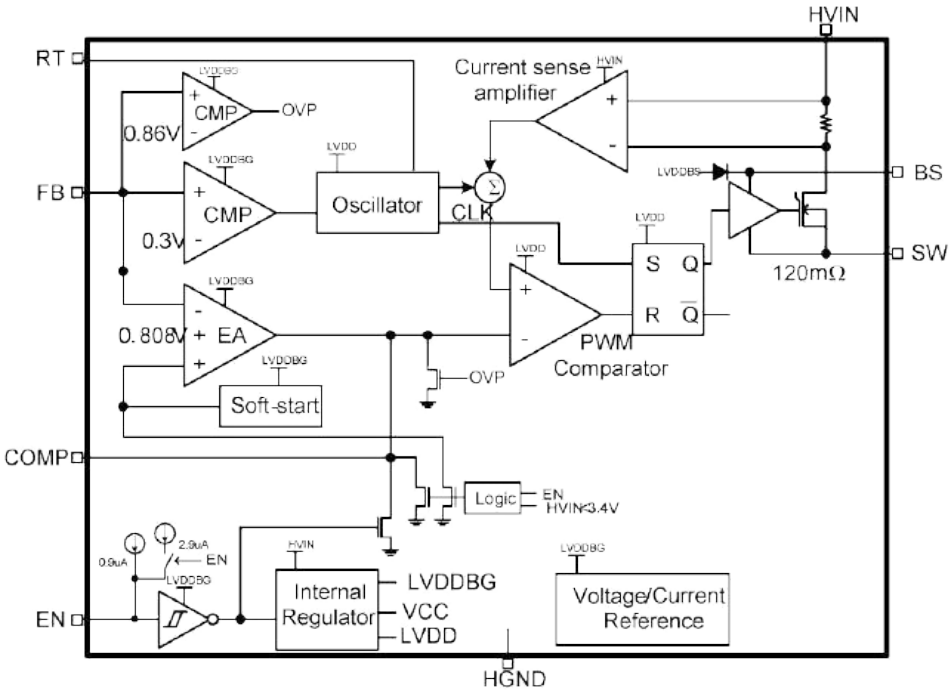


Figure 2. Functional Block Diagram of VPE2503

Absolute Maximum Ratings

Devices are subjected to fail if they stay above absolute maximum ratings.

Input Voltage (V_{IN}) ..... –0.3V to +42V
Switch Voltage (SW) ..... –0.3V to V_{IN}+0.3V
Switch Voltage (SW, 10ns transient) .... –1.4V to V_{IN}+0.3V
Boost Voltage (BS) ..... V_{SW}–0.3V to V_{SW}+7.3V
Enable Voltage (EN) ..... –0.3V to V_{IN}
All Other Pins (RT, FB, COMP) ..... –0.3V to +6V
Lead Temperature (Soldering, 10 sec) ..... 260°C
Junction Temperature (Note 1) ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
ESD Susceptibility HBM 2KV
ESD Susceptibility MM 200V

Recommended Operating Conditions

Input Voltage (V_{IN}) ..... +4.5V to +36V
Junction Operating Temperature ..... –40°C to 125°C

Thermal Data

Package	Thermal Resistance	Parameter	Value
E-SOP-8L	θ_{JA} (Note 2)	Junction-to-ambient	50°C/W
	$\theta_{JC(top)}$ (Note 3)	Junction-case (top)	39°C/W
	$\theta_{JC(bottom)}$ (Note 4)	Junction-case (bottom)	10°C/W
TDFN-10L	θ_{JA} (Note 2)	Junction-to-ambient	55°C/W
	$\theta_{JC(top)}$ (Note 3)	Junction-case (top)	34.7°C/W
	$\theta_{JC(bottom)}$ (Note 4)	Junction-case (bottom)	3.2°C/W

Electrical Characteristics

V_{IN}=12V, T_A=+25°C, unless otherwise specified.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Feedback Voltage	V_{FB}	4.5V≤V_{IN}≤36V	0.788	0.808	0.828	V
Switch on Resistance	$R_{DS(ON)}$	-	-	120	180	mΩ
High-side Switch Leakage	I_{SW}	V_{EN}=0V, V_{SW}=0V	-	-	10	μA
Current Limit	I_{LIM}	F_{OSC}=200kHz	-	4.5	-	A
COMP to Current Sensing Transconductance	G_{CS}	Note 5	-	9	-	A/V
Error Amplifier Voltage Gain	A_{EA}	Note 5	-	200	-	V/V
Error Amplifier Transconductance	G_{EA}	I_{COMP}=±3μA (Note 5)	-	68	-	μA/V
Error Amplifier Min Source Current	-	FB=0.7V	-	5	-	μA
Error Amplifier Min Sink Current	-	FB=0.9V	-	-5	-	μA
VIN UVLO Threshold	V_{UVLO}	-	3.9	4.2	4.5	V
VIN UVLO Hysteresis	-	-	-	800	-	mV
Oscillation Frequency	F_{OSC}	V_{FB}=0.6V; RT=200kΩ	400	500	600	kHz
Fold-Back Frequency	-	V_{FB}=0V; RT=200kΩ	50	125	175	kHz
Shutdown Supply Current	I_{SD}	V_{EN}=0	-	10	20	μA
Quiescent Supply Current	I_Q	V_{EN}=2V, No load, switching supply current	-	0.6	0.8	mA
	-	V_{EN}=2V, V_{FB}=1V, nonswitching supply current	-	0.5	0.7	mA
Thermal Shutdown	T_{SD}	-	-	150	-	°C
Thermal Shutdown Hysteresis	-	-	-	20	-	°C
Minimum Off Time	T_{OFF}	Note 5	-	200	-	ns
Minimum On Time	T_{ON}	Note 5	-	100	-	ns
EN Input Low Voltage	-	-	-	-	0.4	V
EN Input High Voltage	-	-	1.2	-	-	V

- **Note 1:** T_J is a function of the ambient temperature T_A and power dissipation P_D ($T_J = T_A + ((P_D) * \theta_{JA})$).
- **Note 2:** θ_{JA} is simulated in the natural convection at T_A=25°C on a highly effective thermal conductivity (thermal land area completed with >3*3cm^2 area) board (2 layers , 2S0P) according to the JEDEC 51-7 thermal measurement standard.
- **Note 3:** $\theta_{JC(top)}$ represents the heat resistance between the chip junction and the top surface of package.
- **Note 4:** $\theta_{JC(bottom)}$ represents the heat resistance between the chip junction and the center of the exposed pad on the underside of the package.
- **Note 5:** Guaranteed by design.

Typical Performance Characteristics

V_{IN}=12V, V_{OUT}=5.0V, T_A=25°C, unless otherwise specified.

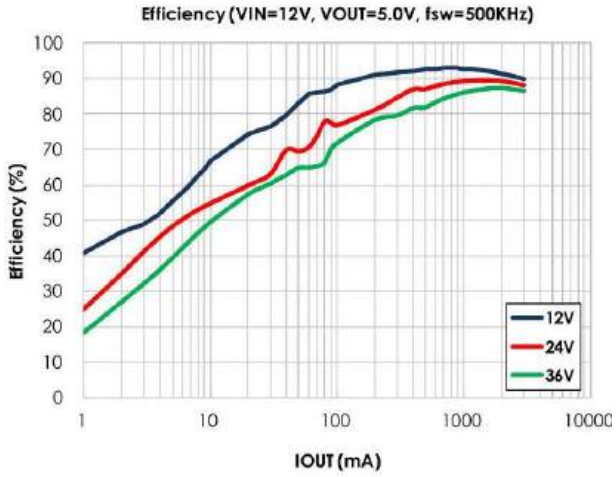


Figure 3. Efficiency vs. Output Current

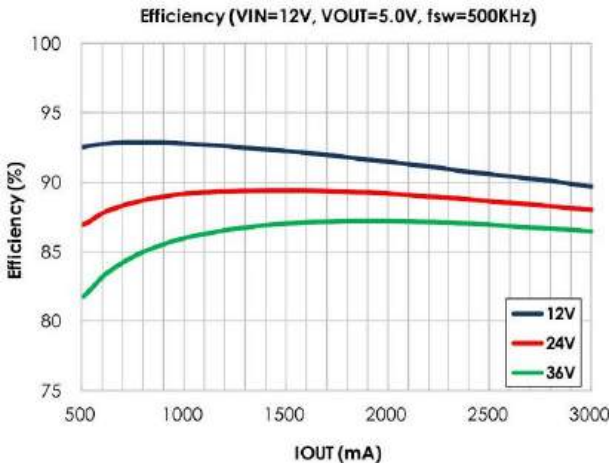


Figure 4. Efficiency vs. Output Current (High Load)

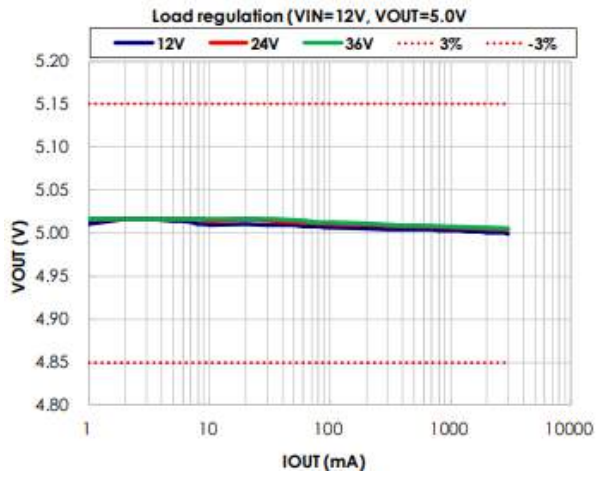


Figure 5. Line Regulation

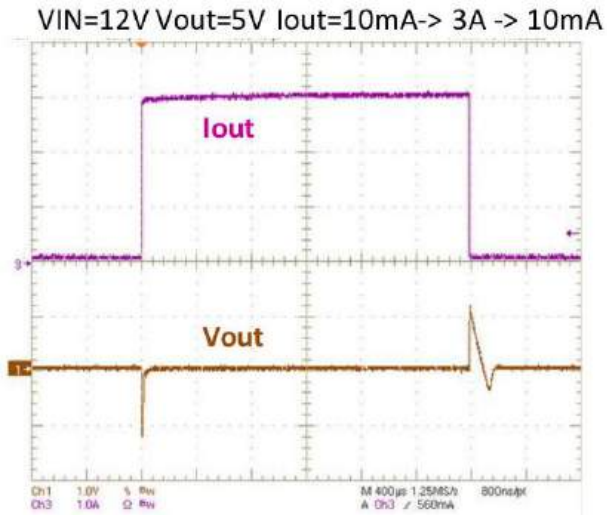


Figure 6. Load Transient

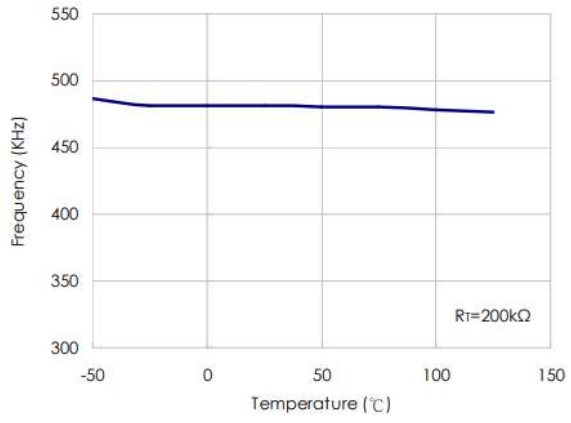


Figure 7. Oscillator Frequency vs. Temperature

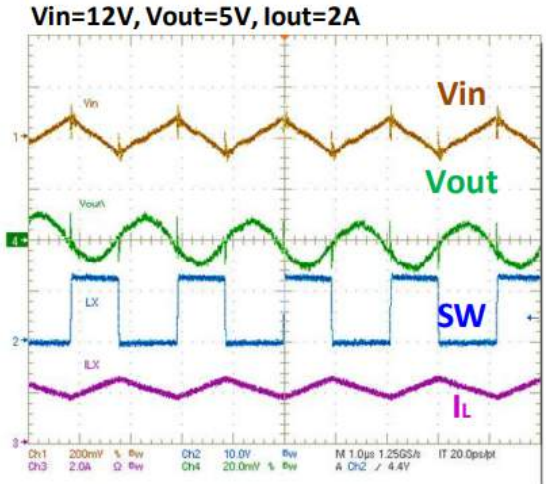


Figure 8. Input/Output Ripple Voltage

Typical Performance Characteristics (Cont.)

V_{IN}=12V, V_{OUT}=3.3V, T_A=25°C, unless otherwise specified.

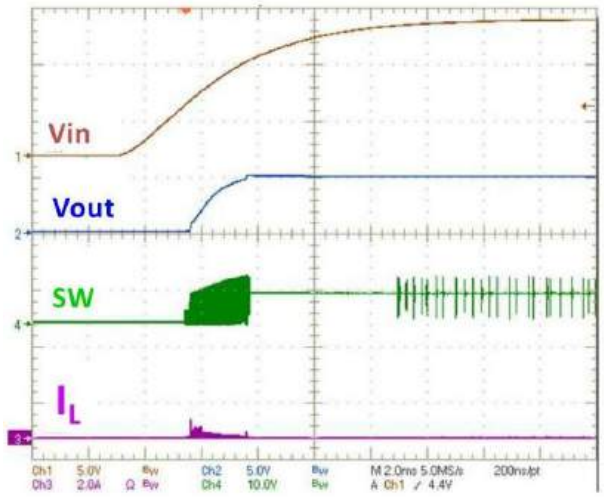


Figure 9. Power Up Without Load

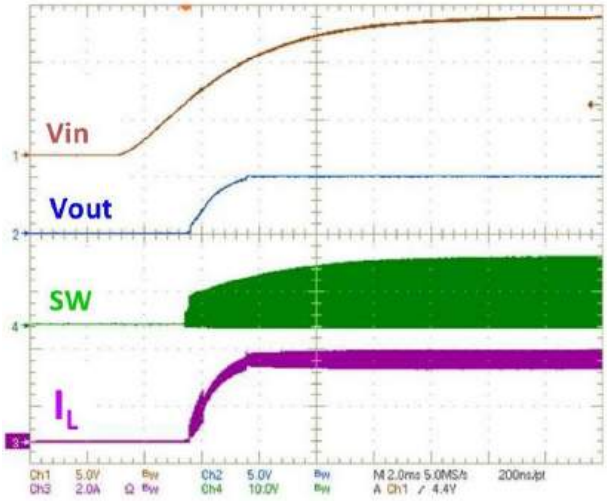


Figure 10. Power Up With 3A Load

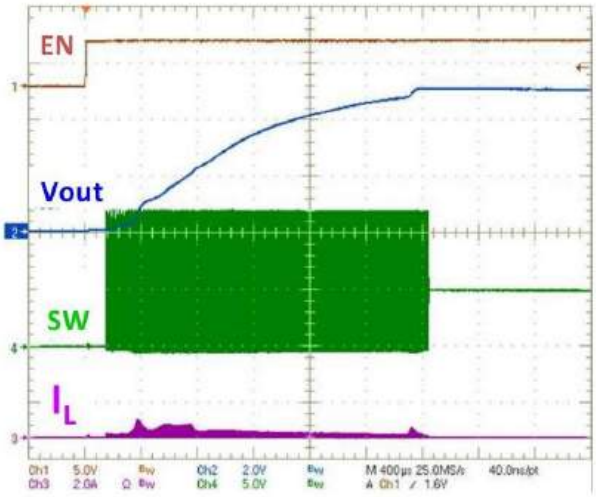


Figure 11. Enable Startup at No Load

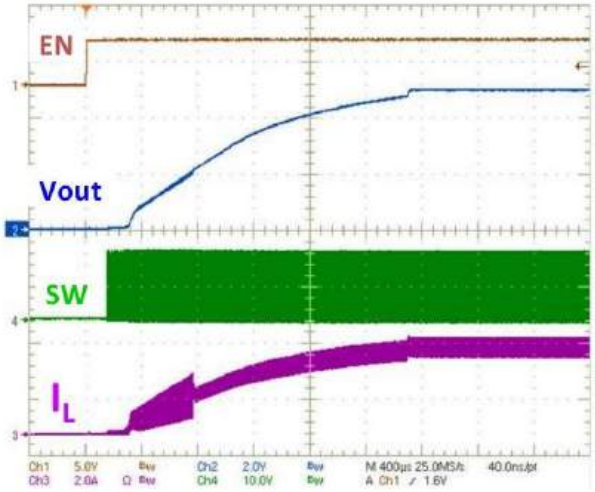


Figure 12. Enable Startup at Full Load

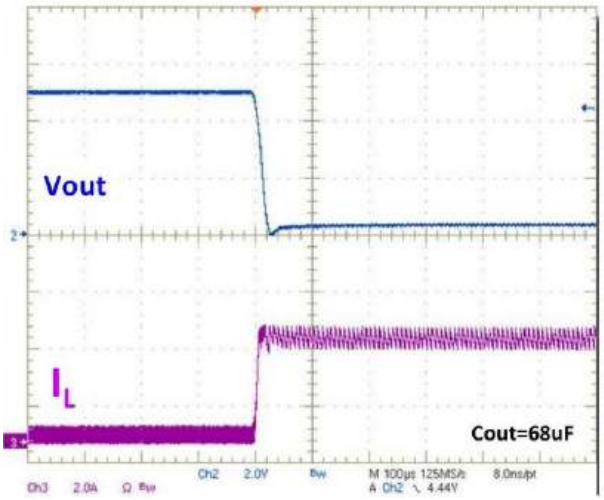


Figure 13. Vout Short Waveform

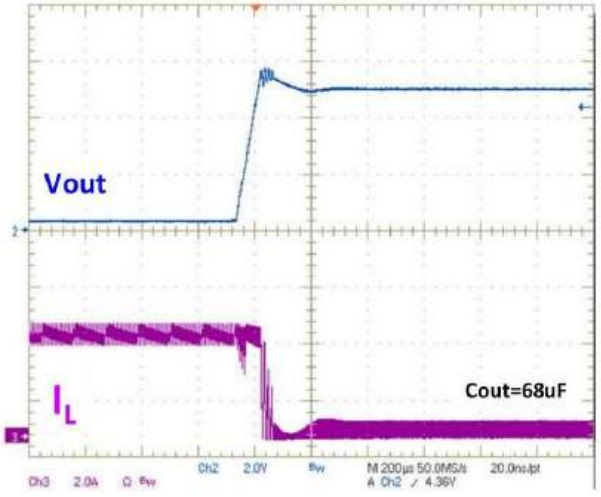


Figure 14. Short Release Waveform

Detailed Description

The VPE2503 is a variable frequency, current mode, automotive buck converter with an integrated high-side switch. The device operates with input voltages from 4.5V to 36V and tolerates input transients up to 42V. During light-load conditions, the device enters Pulse Skip Mode, automatically.

Wide Input Voltage Range (4.5V to 36V)

The VPE2503 includes two separate supply inputs, VIN and BS, specified for a wide 4.5V to 36V input voltage range. VIN provides power to the device and BS provides power to the internal high-side switch driver. With respect to PWM minimum duty limit in VPE2503, the safe operating voltage area shall be considering in here. The Safe Operating Voltage Area (SOVA) is showed in the Fig.15.

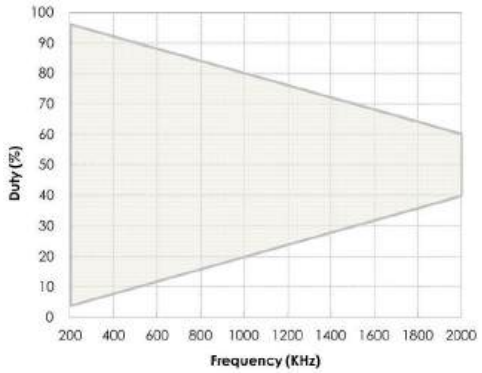


Fig.15 VPE2503 Safe Operating Voltage Area

Error Amplifier

The error amplifier compares the FB pin voltage with the internal 0.808V reference and outputs a current proportional to the difference between the two. This output current is then used to charge or discharge the external compensation network on COMP pin to form the COMP voltage, which is used to control the power MOSFET current. During operation, the COMP voltage is range from 0.2V to 2.0V. COMP is internally pulled down to GND in shutdown mode. The voltage over 2.6V on COMP pin is not allowed due to 2.6V internal power.

Minimum On-Time

The device features a 100ns minimum on-time that ensures proper operation at high switching frequency and high differential voltage between the input and the output.

Enable Control

The VPE2503 has a dedicated enable control pin, EN. By pulling it high or low, that can be enabled and disabled. Tie EN to IN through a 100kΩ resistor for automatic start up. To disable the part, EN must be pulled low for at least 5us. When floating, EN is pulled up to about 2.0V by an internal 1uA current source so it is enabled. To pull it down, >10uA current capability is needed.

Over-Temperature Protection

Thermal overload protection limits the total power dissipation in the device. When the junction temperature exceeds 150°C, an internal thermal sensor shuts down the whole chip. The thermal sensor turns on the IC again after the junction temperature is cooled by 20°C.

Under Voltage Lock-out (UVLO)

UVLO is implemented to protect the chip from operating at insufficient supply voltage. The UVLO rising threshold is about 4.2V while its falling threshold is about 3.4V. If a higher UVLO is required for a specified application, as the EN pin shown in Fig.16 below to adjust input voltage UVLO via two external resistors and a filter capacitor.

The EN enable threshold is around 1.0V (EN_{ON}), and with 100mV hysteresis window (EN_{OFF}) for shutdown. An internal pull-up current source I_E (0.9uA) is in default operating when EN pin floats. Once the EN pin voltage exceed the EN_{ON}, an additional 2.9μA of hysteresis, I_H, is added. This additional current facilitates adjustable input voltage UVLO hysteresis. Use Equation (a) to set the external UVLO hysteresis voltage. Use Equation (b) to set the external UVLO start voltage. For example, choosing R_3=330kΩ and R_4=43kΩ, the external UVLO V_{UVLO_start} and V_{UVLO_stop} would be around 9V and 7V.

$$R_3 = \frac{V_{UVLO\_start} - k\,V_{UVLO\_stop}}{k\,3.8\mu - 0.9\mu} \quad \text{.....(a)}$$

$$R_4 = \frac{EN_{on}}{\frac{V_{UVLO\_start} - EN_{on}}{R_3} + 0.9\mu} \quad \text{.....(b)}$$

$$k = \frac{EN_{on}}{EN_{off}} = 1.1$$

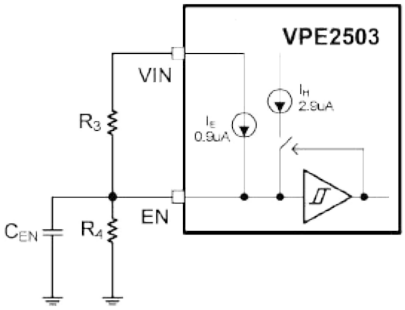


Fig.16 External UVLO Lock-out

Boost Capacitor

Connect a 1uF capacitor between the BS pin and SW pin. This capacitor provides the gate driver voltage for the high-side MOSFET. Also, an UVLO in the floating supply is implemented to protect the high-side MOSFET and its driver from operating at insufficient supply voltage. The UVLO rising threshold is about 2.2V while its hysteresis is about 0.16V.

Over-Current Protection

Over-current limiting is implemented by sensing the drain-to-source voltage across the high-side MOSFET. The drain to source voltage is then compared to a voltage level representing the over-current threshold limit. If the drain-to-source voltage exceeds the over-current threshold limit, the over-current indicator is set true. Once over-current indicator is set true, over-current limiting is triggered. The high-side MOSFET is turned off for the rest of the cycle. The output voltage will start to drop if the output is dead-short to ground, suddenly. Once the FB is lower than 0.3V, the switching frequency of VPE2503 is folded back to around 1/4 f_{SW}.

Over-Voltage Protection

The VPE2503 is with an output voltage protection circuit to minimize output voltage overshoot when fast unload transients or fast supply transients or recovering from overloaded conditions, especially in application design with high inductance and low output capacitance. If the FB pin voltage is rising over 108% of reference voltage (V_{ref}=0.808V), the high side MOS is turned-off immediately. When the FB pin voltage drops below 104% of reference voltage, the high side MOS goes to normal operation.

Although there is an output overvoltage protection, the overshooting voltage would still be seen in designs with improper inductance (L) and output capacitance (C_{out}) due to the energy stored in inductor transfer to output capacitor. For example with V_O=5V, the output protection voltage $V_{O,OVP}$=5.4V, the output overshoot voltage $V_{overshoot}$ would be around 7.35V during a fast load transient current (i) from 5A to 1mA with L=22uH and C_{out}=22uF. But with the same fast load transient, the output overshoot voltage would be down to around 5.62V with L=10uH and C_{out}=100uF. The value of output overshoot voltage $V_{overshoot}$ can be calculated from:

$$V_{overshoot} = \sqrt{\frac{L}{C_{out}} i^2 + V_{O,OVP}^2}$$

Programmable Oscillator

The VPE2503 oscillating frequency (200kHz∼2MHz adjustable switching frequency) is set by an external resistor, R_T from the RT pin to GND. The value of R_T can be calculated from:

$$\text{Frequency(kHz)} = \frac{7.5\,10^4}{R_T^{0.945}(\text{k}\Omega)}$$

Application Information

The schematic on the front page shows a typical application circuit. The IC can provide up to 3A output current at a 3.3V output voltage. For proper thermal performances, the exposed pad of the device must be soldered down to the PCB.

Setting the Output Voltage

The output voltage is set by the resistive voltage divider from the output voltage to FB pin. The voltage divider divides the output voltage down to the feedback voltage by the ratio:

$$V_{FB} = V_{OUT} \frac{R_2}{R_1 + R_2} \Rightarrow V_{OUT} = V_{FB} \frac{R_1 + R_2}{R_2}$$

Table 1. Resistor Selection for Common Output Voltages

V_{OUT}	R1 (kΩ)	R2 (kΩ)
1.8V	33.1 (1%)	27 (1%)
2.5V	50.2 (1%)	24 (1%)
3.3V	37 (1%)	12 (1%)
5.0V	62.3 (1%)	12 (1%)
12V	277 (1%)	20 (1%)

Selecting the Inductor

The common rule for determining the inductance to use is to allow the peak-to-peak ripple current in the inductor to be between 20% and 40% of the DC maximum load current, typical 30%. And also have sufficiently high saturation current rating and a DCR as low as possible. Generally, it is desirable to have lower inductance in switching power supplies, because it usually corresponding to faster transient response, smaller DCR and reduced size for more compact designs. But too low of an inductance results in higher ripple current such that over-current protection at full load could be falsely triggered. Also, the output ripple voltage and efficiency become worse with lower inductance. Under light load condition, like below 100mA, larger inductance is recommended for improved efficiency. The inductance and its peak current could be calculated by:

$$L = \frac{V_{OUT}}{f_S \Delta I_L} \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

$$I_{LP} = I_{LOAD} + \frac{\Delta I_L}{2} = I_{LOAD} + \frac{V_{OUT}}{2 f_S L} \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Which f_S is the switching frequency; I_{LOAD} is the load current.

Table 2. Inductor Selection Guide

Model	I_{SAT} (A)	DCR (mΩ)	Manufacture
PCM104T-100MS	8.5	27 (typ.)	CYNTEC

Selecting the Diode

The diode connected between SW and GND is the path for the inductor current during the high-side MOSFET turns off. Choose the diode with minimum forward voltage drop and recovery time, like Schottky. And, the reverse voltage rating is greater than maximum input voltage and whose current rating is greater than the maximum load current.

Table 3. Diode Selection Guide

Diode	Voltage/Current Rating	Manufacture
B340C	40V, 3A	Diodes Inc.

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current for step-down converter to maintain the DC input voltage. Use low ESR capacitor for the best performance. The high frequency impedance of the capacitor should be lower than the input source impedance for bypassing the high frequency switching current locally. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. To prevent excessive voltage ripple at input, the relationship between the input ripple and the capacitance could be estimated by:

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S C_{IN}} \frac{V_{OUT}}{V_{IN}} \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

For 3A output applications, four 4.7uF ceramic capacitors are sufficient. For V_{IN}¡6V application, the recommended C_{IN} would be 22uF*4.

Selecting the Output Capacitor

The output capacitor (C_O) is required to maintain the DC output voltage, keeps the output ripple small, and ensures regulation loop stability. The lower ESR capacitors are preferred to keep lower output ripple. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S L} \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \left(R_{ESR} + \frac{1}{8 f_S C_O}\right)$$

Which L is the inductance and R_{ESR} is the equivalent series resistance (ESR) of the output capacitor.

In case of lower ESR capacitor adopted, the output ripple is mainly caused by the capacitance and the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 f_S^2 L C_O} \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Or, the ESR dominates the impedance at switching frequency. After simplification, the output voltage ripple can approximated to

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S L} \left(1 - \frac{V_{OUT}}{V_{IN}}\right) R_{ESR}$$

The characteristics of the output capacitor also affect the loop stability of regulation system. Low ESR ceramic capacitors with X5R or X7R dielectrics are recommended.

Compensation Components

The EML3193B employs current mode control for easy compensation and fast transient response. The system stability and transient response are controlled through the COMP pin. COMP pin is the output of the internal error amplifier. A series capacitor-resistor combination sets a pole-zero combination to control the characteristics of the control system. The DC gain of the voltage feedback loop is given by:

$$A_{VDC} = R_L G_{CS} A_{EA} \frac{V_{FB}}{V_O}$$

Where R_L is the load resistor value, G_{CS} is the current sensing transconductance and A_{EA} is the error amplifier gain. The system has two important poles. One is due to the compensation capacitor (C_{CMP}) and the output resistor (r_O) of error amplifier, and the other is due to the output capacitor (C_O) and the load resistor (R_L). These poles are located at:

$$f_{p1} = \frac{1}{2\pi C_{CMP} r_O} = \frac{G_{EA}}{2\pi C_{CMP} A_{VEA}}$$

$$f_{p2} = \frac{1}{2\pi C_O R_L}$$

Where, G_{EA} is the error amplifier transconductance.

The system has one important zero, due to the compensation capacitor (C_{CMP}) and the compensation resistor (R_{CMP}). The zero is located at:

$$f_{Z1} = \frac{1}{2\pi C_{CMP} R_{CMP}}$$

The system may have another important zero, if the output capacitor has a large capacitance with a high ESR value. The zero, due to the ESR and a capacitance of the output capacitor, is located at:

$$f_{ESR} = \frac{1}{2\pi C_O R_{ESR}}$$

In this case, a third pole set by the compensation capacitor (C_C) which is directly connected to COMP Pin between GND and the compensation resistor (R_{CMP}) is used to compensate the effect of the ESR zero(f_{ESR}) on the loop gain. This pole is located at:

$$f_{p3} = \frac{1}{2\pi C_C R_{CMP}}$$

To shape the converter transfer function for getting an adequate loop gain is the purpose of compensation design. The system open loop unity gain crossover frequency is important.

Lower crossover frequencies result in slower line and load transient responses, while higher crossover frequencies could system unstable. A good compromise is to set the crossover frequency to below one-tenth of the switching frequency. To optimize the compensation components, the following procedure can be used:

1. Choose the compensation resistor (R_{CMP}) to set the desired crossover frequency. Determine the R_{CMP} value by the following equation:

$$R_{CMP} = \frac{2\pi C_O f_C}{G_{EA} G_{CS}} \frac{V_O}{V_{FB}}$$

Where, f_C is the desired crossover frequency.

2. Choose the compensation capacitor (C_{CMP}) to get the desired phase margin. For applications with typical inductor values, setting the compensation zero, f_{Z1}, to below one-fourth of the crossover frequency provides sufficient phase margin. Determine the C_{CMP} value by the following equation:

$$C_{CMP} > \frac{4}{2\pi R_{CMP} f_C}$$

Where, R_{CMP} is the compensation resistor value.

To avoid the output voltage unstable due to the parasitic capacitor between the COMP pin and GND, the C_{CMP}¿100pF is strongly recommended.

3. Determine if the second compensation capacitor (C_C) is required. It is required if the ESR zero of the output capacitor is located at less than half of the switching frequency, the following relationship is valid:

$$\frac{1}{2\pi C_O R_{ESR}} < \frac{f_S}{2}$$

If this is the case, then add the second compensation capacitor C_C to set the pole f_{p3} at the location of the ESR zero. Determine the C_C value in the following equation:

$$C_C > \frac{C_O R_{ESR}}{R_{CMP}}$$

And, a 3∼5pF capacitance is suggested to improve full range operating.

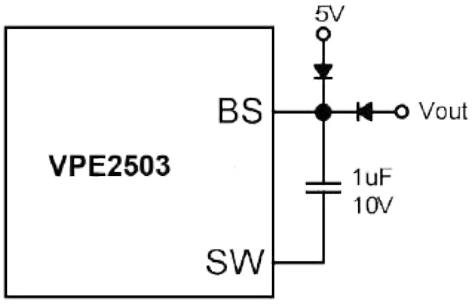
Table 4. Components Selection Guide

V_{OUT} (V)	L (μH)	C_O (μF)	R_{CMP} (kΩ)	C_{CMP} (pF)	C_C (pF)
1.8	4.7	47	36	470	3∼5
2.5	4.7∼6.8	20	27	470	3∼5
3.3	6.8∼10	20	33	470	3∼5
5.0	10∼22	20	50	330	3∼5
12	22∼33	20	91	220	3∼5

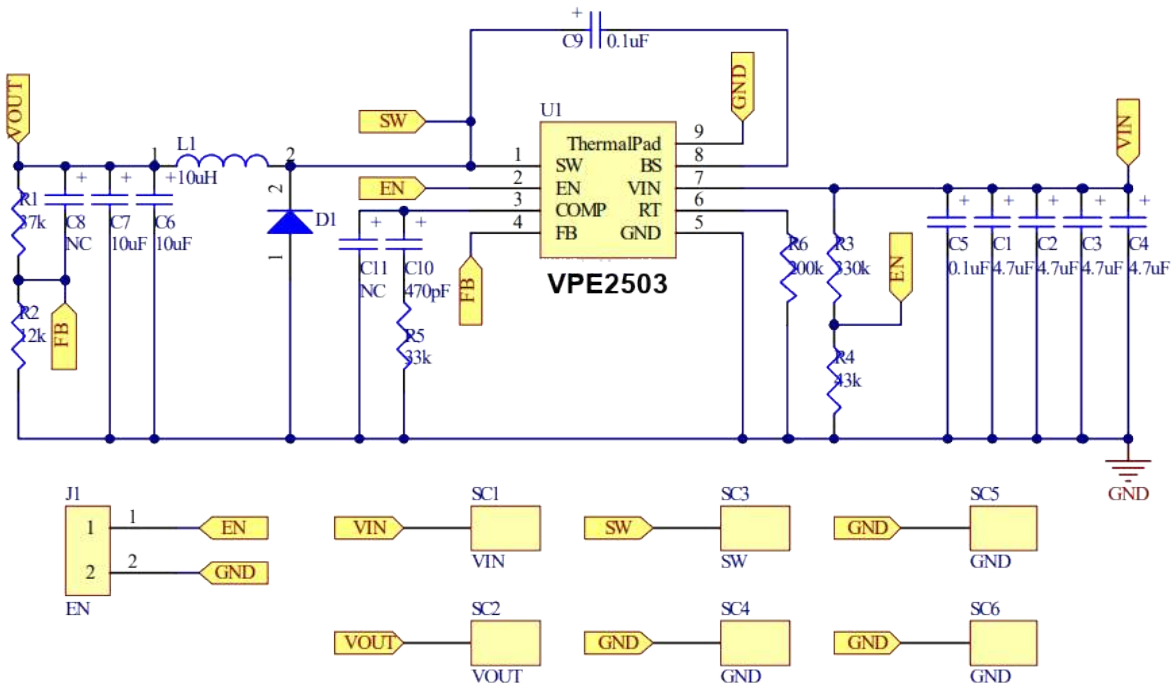
4. The estimation is based on 15% of Iout current for this table. User can calculate it depend on peak-to-peak ripple current real requirement.

External Bootstrap Diode

An external bootstrap diode is recommended to add between external 5V and BS pin to enhance efficiency of the regulator. The external 5V can be a 5V fixed input from system or a 5V output of the EML3193B. The low cost diode, like 1N4148, is sufficient. With such diode, 5V input voltage can output 3.3V and 2.5V with just 30mA load.

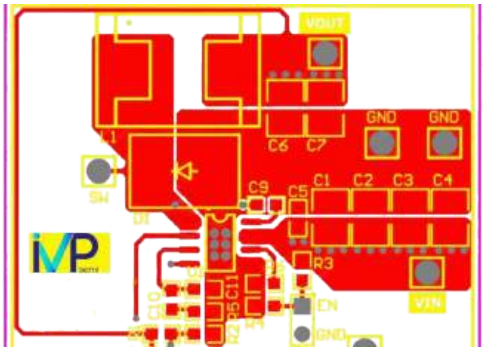


Applications

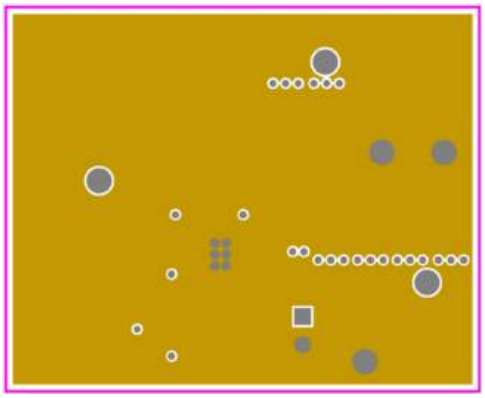


Typical Schematic for PCB Layout

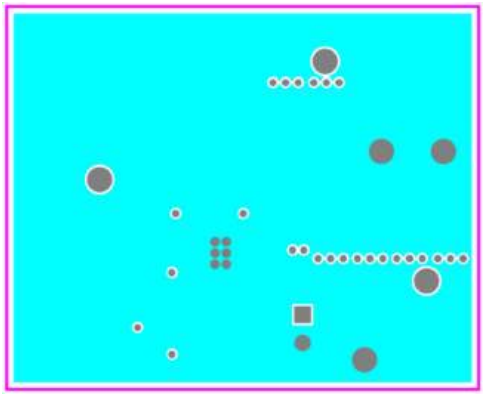
PCB Layout



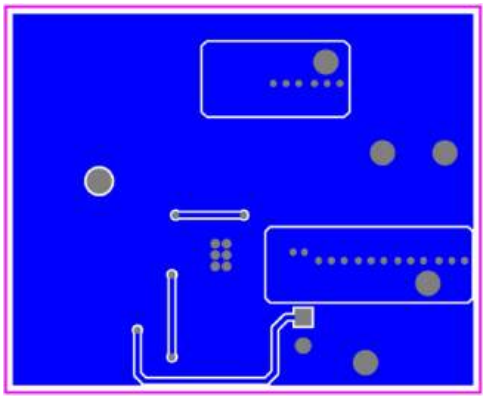
Top-Side Layer Layout



Middle-1 Layer Layout

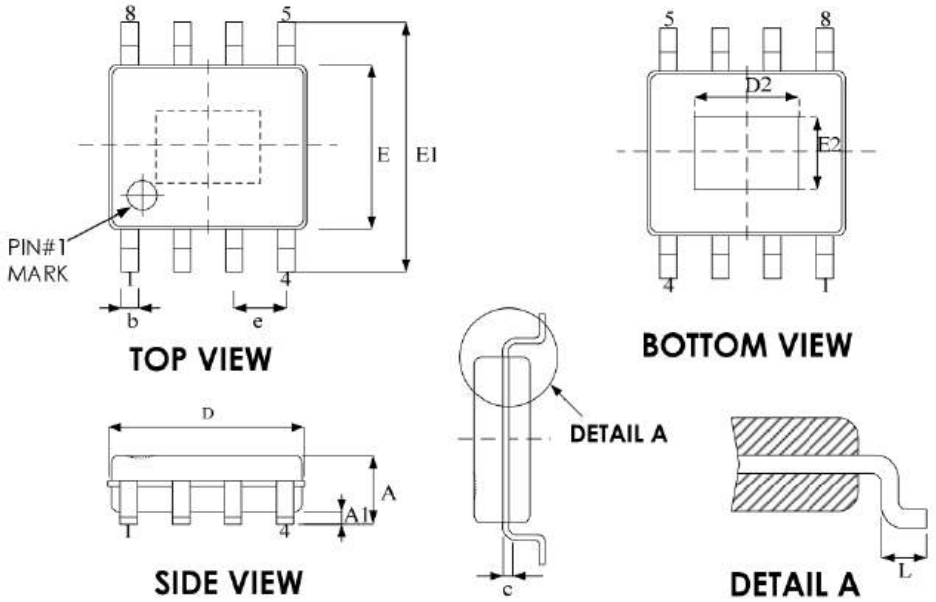


Middle-2 Layer Layout



Bottom-Side Layer Layout

Package Outline Drawing (E-SOP-8L)

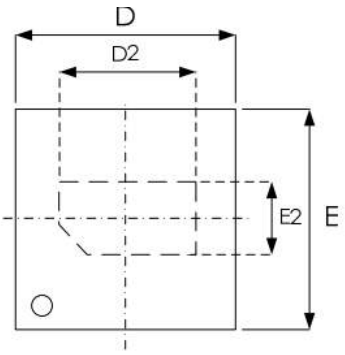


Symbol	Dimension in mm	
	Min.	Max.
A	-	1.70
A1	0.00	0.15
b	0.31	0.51
c	0.10	0.25
D	4.80	5.00
E	3.81	4.00
E1	5.79	6.20
e	1.27 BSC	
L	0.40	1.27

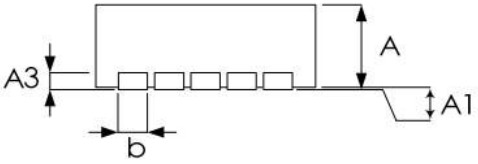
Exposed pad

Symbol	Dimension in mm	
	Min.	Max.
D2	2.80	3.50
E2	2.00	2.60

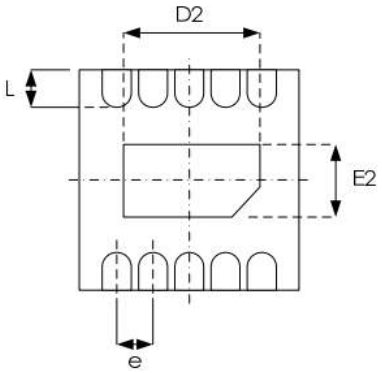
Package Outline Drawing (TDFN-10L)



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Symbol	Dimension in mm	
	Min.	Max.
A	0.70	0.85
A1	0.00	0.05
A3	0.18	0.25
b	0.18	0.30
D	2.90	3.10
E	2.90	3.10
e	0.5 BSC	
L	0.30	0.50

Exposed pad

Symbol	Dimension in mm	
	Min.	Max.
D2	2.20	2.70
E2	1.40	1.75

Disclaimer

The information provided in this datasheet is believed to be accurate and reliable. Errors or omissions are expected. indiaVP Semiconductor Pvt. Ltd. reserves the right to make changes to the product specifications without prior notice. Users should verify the suitability of the product for their specific applications. Please visit our website for the latest datasheet.

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