Description

The VPE2019 features ultra-high power supply rejection ratio, low output voltage noise, low dropout voltage, low quiescent current and fast transient response. It guarantees delivery of 300mA output current and supports preset output voltages ranging from 0.8V to 4.0V with 0.1V increment.

Based on its low quiescent current consumption and its less than 1μA shutdown mode of logical operation, the VPE2019 is ideal for battery-powered applications. The high power supply rejection ratio of the VPE2019 holds well for low input voltages typically encountered in battery-operated systems. The regulator is stable with small ceramic capacitive loads.

The VPE2019 is available in uDFN-4 package.

Key Features

- AEC-Q100 qualified
- 300mA guaranteed output current
- 75dB typical PSRR at 1kHz
- 260mV (V_{OUT}=3.3V) typical dropout at 300mA
- 52μA typical quiescent current
- Less than 1μA typical shutdown mode
- Fast line and load transient response
- 1.7V to 5.5V input range
- Auto-discharge during chip disable
- 0.8V to 4.0V output voltage range
- Stable with small ceramic output capacitors
- Fold-back over current protection
- ±1% output voltage tolerance

Applications

- Wireless handsets
- PCMCIA cards
- DSP core power
- Hand-held instruments
- Battery-powered systems
- Portable information appliances

Typical Application

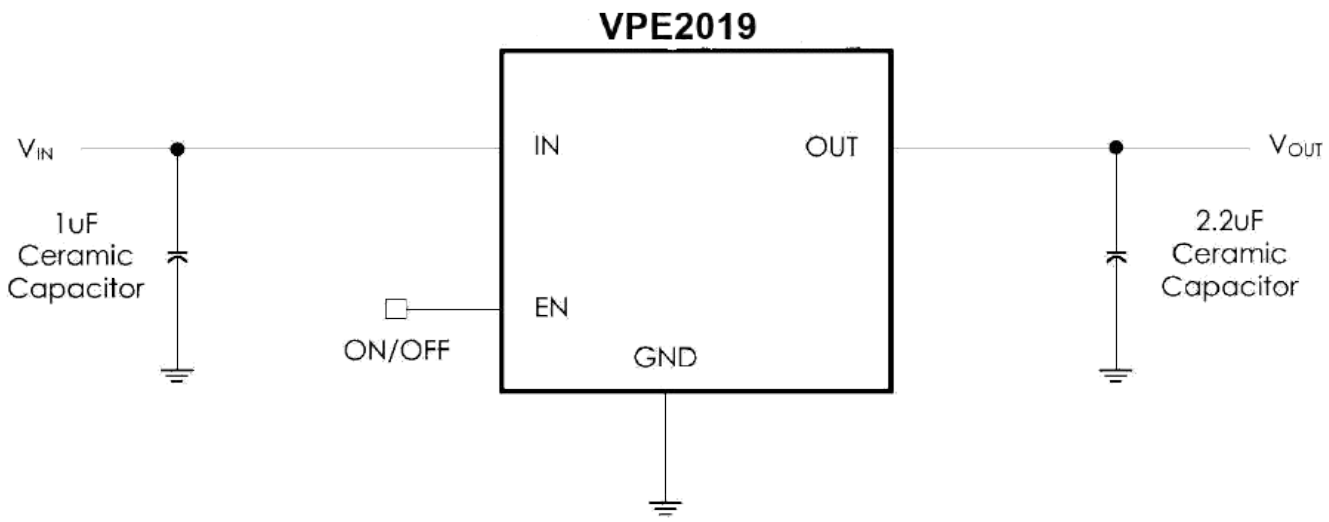
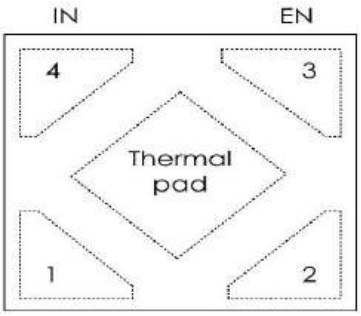


Fig. 1 VPE2019 Typical Application Circuit

Connection Diagrams



uDFN-4

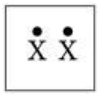
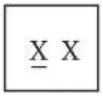
VPE2019-XXFJ04VCR

XX Output voltage

FJ04 uDFN-4 Package

V Automotive Grade
C Rating: -40 to 125℃
R Packing in Tape & Reel

Order, Marking & Packing Information

Package	Vout	Product ID	Marking	Packing
uDFN-4	0.8V	VPE2019-08FJ04VCR (by request)		Tape & Reel, 8Kpcs
	1.0V	VPE2019-10FJ04VCR		
	1.05V	VPE2019-1AFJ04VCR (by request)		
	1.2V	VPE2019-12FJ04VCR		
	1.3V	VPE2019-13FJ04VCR (by request)		
	1.5V	VPE2019-15FJ04VCR (by request)		
	1.8V	VPE2019-18FJ04VCR		
	2.5V	VPE2019-25FJ04VCR (by request)		
	2.8V	VPE2019-28FJ04VCR		
	3.0V	VPE2019-30FJ04VCR		
	3.3V	VPE2019-33FJ04VCR		

XX = tracking code

Pin Functions

Name	uDFN-4	Function
IN	4	**Supply Voltage Input.** Require a minimum input capacitor of close to 1μF ceramic capacitor to ensure stability and sufficient decoupling from the ground pin.
GND	2	**Ground Pin.**
EN	3	**Enable Input.** Enable the regulator by pulling the EN pin High. To keep the regulator on during normal operation, connect the EN pin to V_{IN}. The EN pin must not exceed V_{IN} under all operating conditions.
NC	N/A	**No Connected.**
OUT	1	**Regulated Output Voltage Pin.** A small 2.2μF ceramic capacitor is needed from this pin to ground to assure stability.
Thermal Pad	YES	**Thermal Pad.** The thermal pad with large thermal land area on the PCB will helpful chip power dissipation, to connect it to GND together normally.

Functional Block Diagram

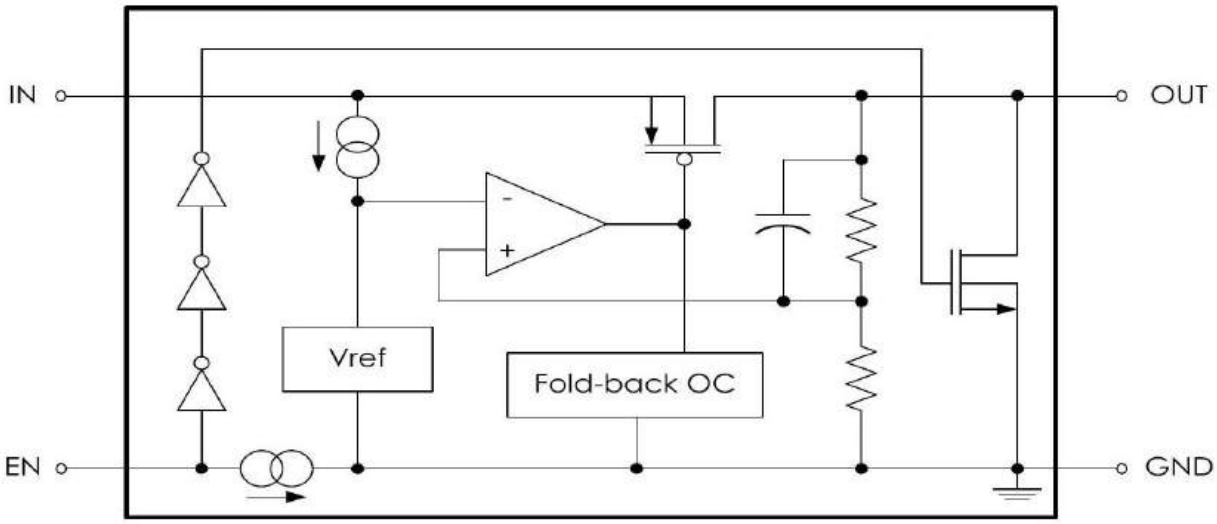


Fig. 2 Functional Block Diagram of VPE2019

Absolute Maximum Ratings

(Notes 1, 2)

IN, EN, OUT ..... –0.3V to 6.5V
Power Dissipation ..... (Note 6)
Storage Temperature Range ..... –65°C to 150°C
Junction Temperature (T_J) ..... 150°C
Lead Temperature (Soldering, 10 sec.) ..... 260°C
ESD Rating (Human Body Model) 2KV
ESD Rating (Charged Device Model) 750V

Operating Ratings

(Notes 1, 2)

Supply Voltage ..... 1.7V to 5.5V
Operating Temperature Range ..... –40°C to 125°C

Thermal Data

Package	Thermal Resistance	Parameter	Value
uDFN-4	θ_{JA} (Note 3)	Junction-to-ambient	110°C/W
	θ_{JC} (Note 4)	Junction-to-case	23°C/W

Electrical Characteristics

Unless otherwise specified, all limits guaranteed for V_{IN} = V_{OUT} + 1V (Note 5), V_{EN} = V_{IN}, C_{IN} = 1μF, C_{OUT} = 2.2μF, T_A = 25°C. Boldface limits apply for the operating temperature extremes: -40°C and 125°C.

Parameter	Symbol	Conditions	Min.	Typ. (Note 7)	Max.	Units
Input Voltage	V_{IN}	-	1.7	-	5.5	V
Output Voltage	V_{OUT}	-	0.8	-	4.0	V
Output Voltage Tolerance	ΔV_{OTL}	V_{OUT} > 2.0V, T=25°C	X0.99	-	X1.01	V
		$V_{OUT} \leq$ 2.0V, T=25°C	-20	-	+20	mV
		V_{OUT} > 2V	**X0.97**	-	**X1.03**	V
		$V_{OUT} \leq$ 2V	**-60**	-	**60**	mV
Maximum Output Current	I_{OUT}	Average DC Current Rating	300	-	-	mA
Current Limit	I_{CL}	V_{IN} = V_{OUT} + 1V	-	420	-	mA
Short Current Limit	I_{SC}	-	-	40	-	mA
Quiescent Current	I_Q	I_{OUT} = 0mA	-	52	75	μA
Shutdown Supply Current	I_{SD}	V_{OUT} = 0V, EN = GND	-	0.2	1	μA
Dropout Voltage						
	V_{DO}	I_{OUT} = 300mA, V_{OUT} = 0.8V	-	860	-	mV
		I_{OUT} = 300mA, V_{OUT} = 1.2V	-	580	-	mV
		I_{OUT} = 300mA, V_{OUT} = 1.5V	-	440	-	mV
		I_{OUT} = 300mA, V_{OUT} = 1.8V	-	380	-	mV
		I_{OUT} = 300mA, V_{OUT} = 2.8V	-	290	-	mV
		I_{OUT} = 300mA, V_{OUT} = 3.3V	-	260	-	mV
Line Regulation	ΔV_{OUT}	I_{OUT} = 1mA, (V_{OUT} + 1V) $\leq V_{IN} \leq$ 5.5V	-	0.02	0.1	%/V
Load Regulation	ΔV_{OUT}	1mA $\leq I_{OUT} \leq$ 300mA	-	10	30	mV
Power supply rejection ratio	PSRR	f = 1kHz, Ripple 0.2 Vp-p, V_{IN} = Set V_{OUT} + 1V, I_{OUT} = 30mA	-	75	-	dB
Output Voltage Noise	e_n	V_{OUT} = 0.8V, I_{OUT} = 30mA, 10Hz $\leq$ f $\leq$ 100kHz	-	40	-	μV_{RMS}
EN Input Threshold	V_{EN}	V_{IH}	1.0	-	-	V
		V_{IL}	-	-	0.4	V
EN Input Bias Current	I_{EN}	EN = GND or V_{IN}	-	0.1	1	μA

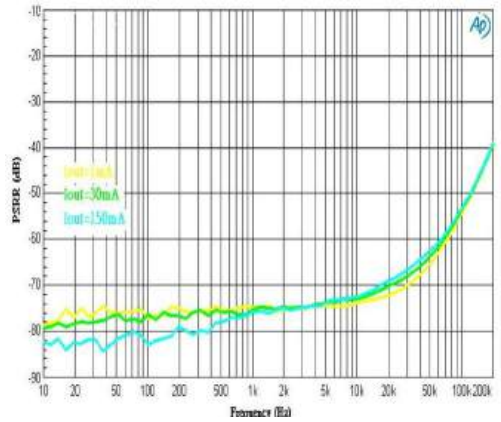
- **Note 1:** Absolute Maximum ratings indicate limits beyond which damage may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions.
- **Note 2:** All voltages are with respect to the potential at the ground pin.
- **Note 3:** θ_{JA} is measured in the natural convection at T_A=25°C on a high effective thermal conductivity test board (2 layers, 2S0P).
- **Note 4:** θ_{JC} represents the resistance to the heat flows the chip to package top case.
- **Note 5:** Dropout voltage is measured by reducing V_{IN} until V_{OUT} drops 100mV from its nominal value at V_{IN} - V_{OUT} = 1V.
- **Note 6:** Maximum Power dissipation for the device is calculated using the following equations:

$$P_D = (T_{J(MAX)} - T_A) / \theta_{JA}$$

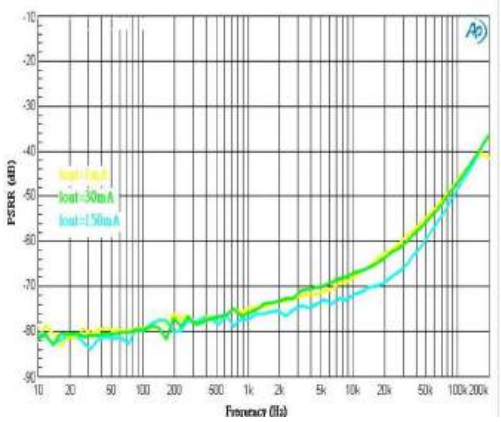
  Where T_J(MAX) is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance. E.g. for the SOT-23-5 package θ_{JA} = 152°C/W, T_J (MAX) = 150°C and using T_A = 25°C, the maximum power dissipation is found to be 0.82W. The derating factor (-1/θ_{JA}) = -6.6mW/°C, thus below 25°C the power dissipation figure can be increased by 6.6mW per degree, and similarity decreased by this factor for temperatures above 25°C.
- **Note 7:** Typical values represent the most likely parametric norm.

Typical Performance Characteristics

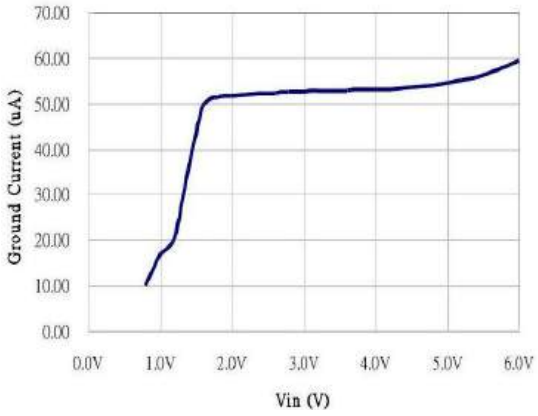
Unless otherwise specified, V_{IN} = $V_{OUT(NOM)}$ + 1V, V_{EN} = V_{IN}, C_{IN} = 1μF, C_{OUT} = 2.2μF, T_A = 25°C



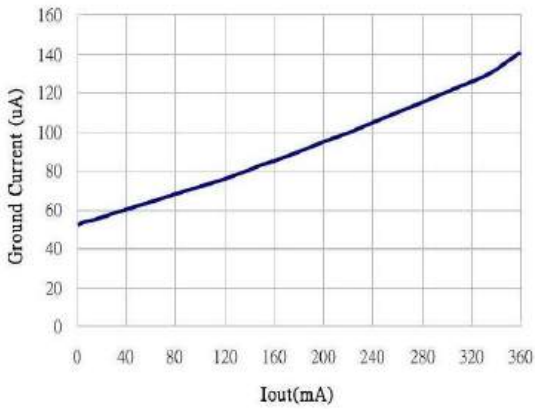
PSRR vs. Frequency (V_{OUT}=0.8V)



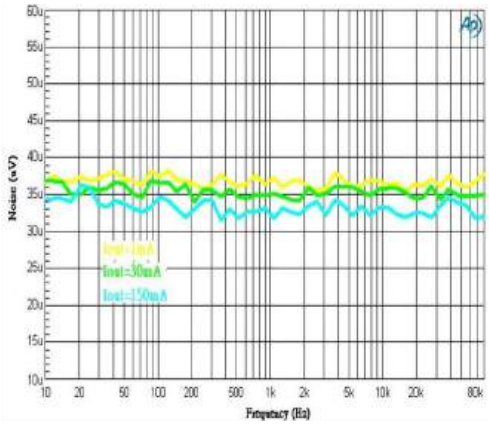
PSRR vs. Frequency (V_{OUT}=3.3V)



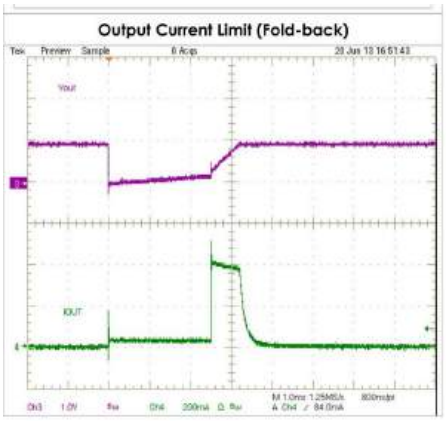
Ground Current vs. V_{IN} (V_{OUT}=0.8V)



Ground Current vs. I_{OUT} (V_{OUT}=0.8V)

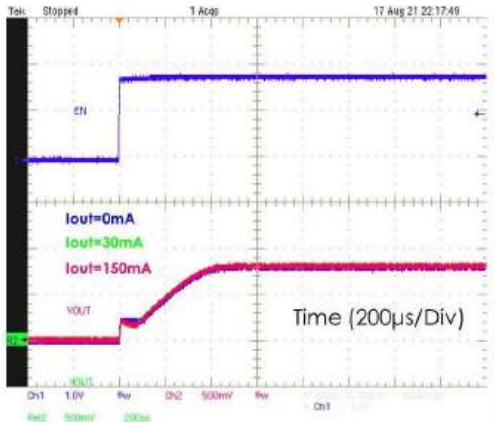


Output Voltage Noise

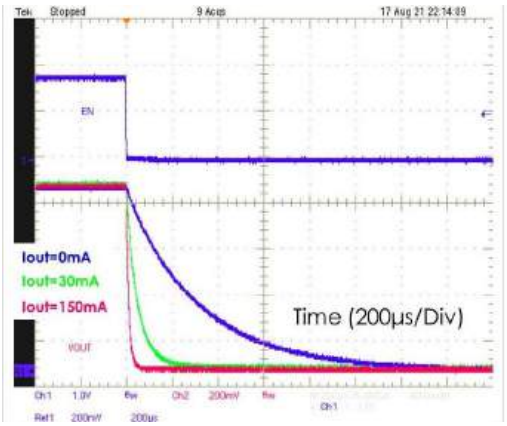


Output Current Limit (Fold-back)

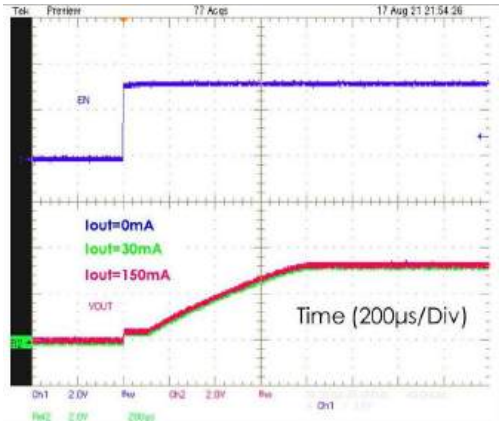
Typical Performance Characteristics (cont.)



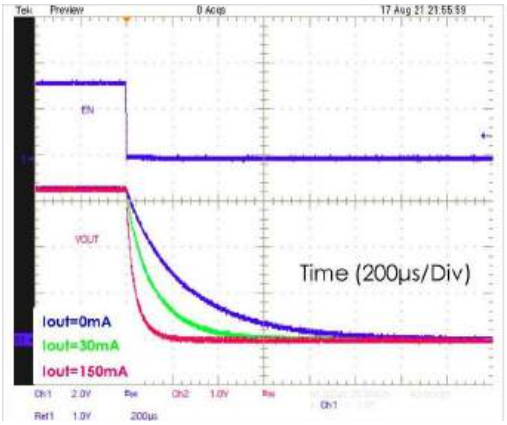
Enable Response (V_{OUT}=0.8V)



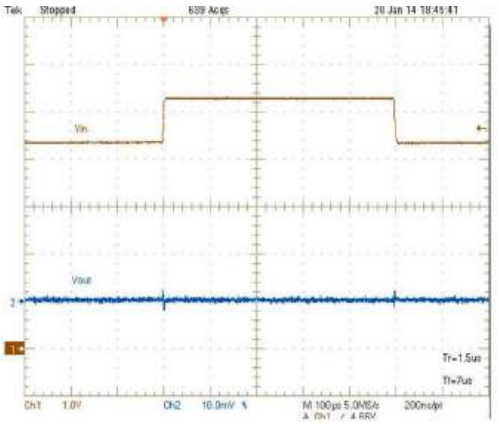
Disable Response (V_{OUT}=0.8V)



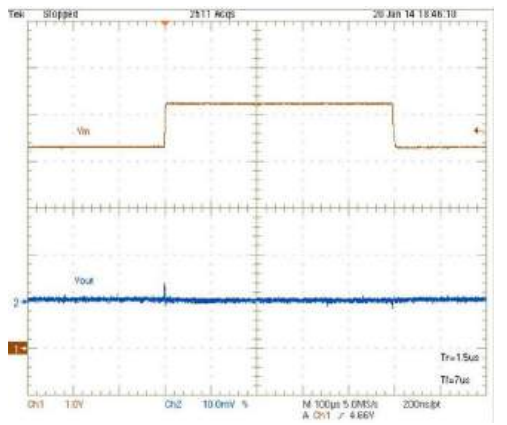
Enable Response (V_{OUT}=3.3V)



Disable Response (V_{OUT}=3.3V)

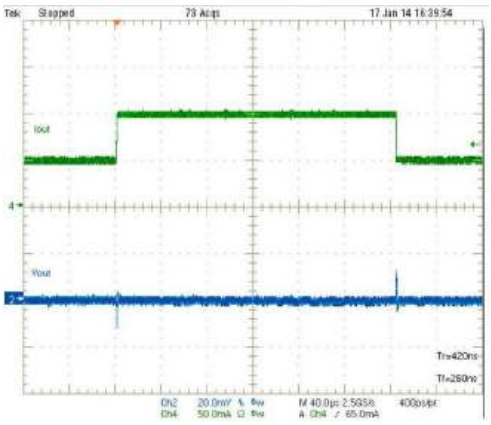


Line Transient (I_{OUT}=30mA, V_{IN}=4.3V~5.3V, V_{OUT}=3.3V)

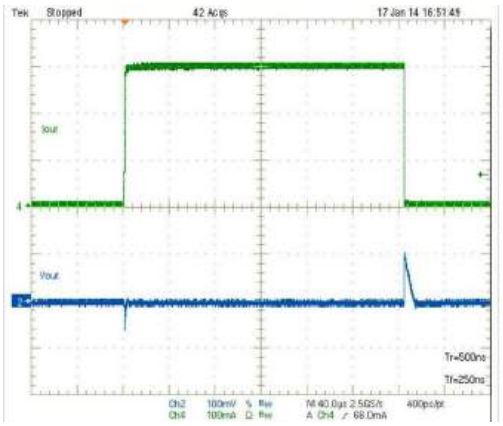


Line Transient (I_{OUT}=300mA, V_{IN}=4.3V~5.3V, V_{OUT}=3.3V)

Typical Performance Characteristics (cont.)



Load Transient (V_{OUT}=0.8V, I_{OUT}=50mA to 100mA)



Load Transient (V_{OUT}=0.8V, I_{OUT}=1mA to 300mA)

Application Information

General Description

Referring to Fig.2 as shown in the Functional Block Diagram section, the VPE2019 adopts the classical regulator topology in which negative feedback control is used to perform the desired voltage regulating function. The sub Vout-select form the feedback circuit which samples the output voltage for the error amplifier's non-inverting input. The inverting input is set to the bandgap reference voltage. Due to its high open-loop gain, the error amplifier ensures that the sampled output feedback voltage at its non-inverting input is virtually equal to the preset voltage reference voltage. The error amplifier compares the voltage difference at its inputs and produces an appropriate driving voltage to the P-channel MOS pass transistor, which controls the amount of current reaching the output. If there are changes in the output voltage due to load changes, the feedback resistors register these changes to the non-inverting input of the error amplifier. The error amplifier then adjusts its driving voltage to maintain virtual short between its two input nodes under all loading conditions. The regulation of the output voltage is achieved as a direct result of the error amplifier keeping its input voltages equal. This negative feedback control topology is further augmented by the shutdown, the temperature and current protection circuitry.

Output Capacitor

The VPE2019 is specially designed for use with ceramic output capacitors of as low as 2.2μF to take advantage of the savings in cost and space, as well as the superior filtering of high frequency noise. Capacitors of higher value or other types may be used, but it is important to make sure its equivalent series resistance (ESR) be restricted to less than 0.5Ω. The use of larger capacitors with smaller ESR values is desirable for applications involving large and fast input or output transients, as well as situations where the application systems are not physically located immediately adjacent to the battery power source. Typical ceramic capacitors suitable for use with the VPE2019 are X5R and X7R. The X5R and the X7R capacitors are able to maintain their capacitance values to within ±20% and ±10%, respectively, as the temperature increases.

No-Load Stability

The VPE2019 is capable of stable operation during no-load conditions, a mandatory feature for some applications such as CMOS RAM keep-alive operations.

Input Capacitor

A minimum input capacitance of 1μF is required for VPE2019. The capacitor value may be increased without limit. Improper workbench set-ups may have adverse effects on the normal operation of the regulator. A case in point is the instability that may result from long supply lead inductance coupling to the output through the gate capacitance of the pass transistor. This will establish a pseudo LCR network, and is likely to happen under high current conditions or near dropout. A 10μF tantalum input capacitor will dampen the parasitic LCR action thanks to its high ESR. However, cautions should be exercised to avoid regulator short-circuit damage when tantalum capacitors are used, for they are prone to fail in short-circuit operating conditions.

Power Dissipation

Thermal overload results from excessive power dissipation that causes the IC junction temperature to increase beyond a safe operating level. The concept of thermal resistance θ_{JA} (°C/W) is often used to describe an IC junction's relative readiness in allowing its thermal energy to dissipate to its ambient air. An IC junction with a low thermal resistance is preferred because it is relatively effective in dissipating its thermal energy to its ambient, thus resulting in a relatively low and desirable junction temperature. The relationship between θ_{JA} and T_J is as follows:

$$T_J = \theta_{JA}(P_D) + T_A \quad \text{(Eq. 1)}$$

T_A is the ambient temperature, and P_D is the power generated by the IC and can be written as:

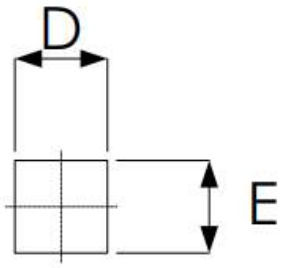
$$P_D = I_{OUT}(V_{IN} - V_{OUT}) \quad \text{(Eq. 2)}$$

As the above equations show, it is desirable to work with ICs whose θ_{JA} values are small such that T_J does not increase strongly with P_D. To avoid thermally overloading the VPE2019, refrain from exceeding the absolute maximum junction temperature rating of 150°C under continuous operating conditions. Overstressing the regulator with high loading currents and elevated input-to-output differential voltages can increase the IC die temperature significantly.

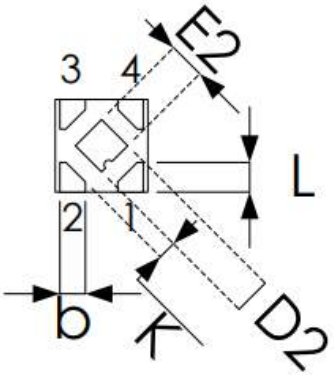
Shutdown

The VPE2019 enters sleep mode when the EN pin is low. When this occurs, the pass transistor, the error amplifier, and the biasing circuits, including the bandgap reference, are turned off, thus reducing the supply current to typically $< 1\mu$A. The low supply current makes the VPE2019 best suited for battery-powered applications. The maximum guaranteed voltage at the EN pin to enter sleep mode is 0.4V. A minimum guaranteed voltage of 1.0V at the EN pin will activate the VPE2019. To constantly keep the regulator on, direct connection of the EN pin to the VIN pin is allowed.

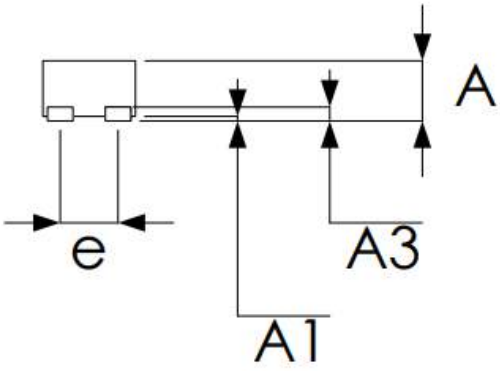
Package Outline Drawing(UDFN1X1-4L (1×1 mm))



TOP VIEW



BOTTOM VIEW



SIDE VIEW

Symbol	Dimension in mm	
	Min.	Max.
A	0.35	0.40
A1	0.00	0.05
A3	0.12 REF	
b	0.175	0.275
D	1.00 BSC	
E	1.00 BSC	
e	0.65 BSC	
L	0.20	0.30
K	0.20 REF	

Exposed Pad

Symbol	Dimension in mm	
	Min.	Max.
D2	0.40	0.60
E2	0.40	0.60

All dimensions are in millimeters.

Disclaimer

The information provided in this datasheet is believed to be accurate and reliable. Errors or omissions are expected. indiaVP Semiconductor Pvt. Ltd. reserves the right to make changes to the product specifications without prior notice. Users should verify the suitability of the product for their specific applications. Please visit our website for the latest datasheet.

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