General Description

The VPE2016 is a high voltage, low quiescent current, low dropout regulator with 150mA output driving capacity. The VPE2016, which operates over an input range of 3V to 32V, is stable with any capacitors, whose capacitance is larger than 1μF, and suitable for powering battery-management ICs because of the virtue of its low quiescent current consumption and low dropout voltage. VPE2016 also includes bandgap voltage reference, fold-back current limiting and thermal overload protection.

Key Features

- AEC-Q100 qualified
- 150mA output current driving capacity
- 780mV typical dropout at Io=150mA@V_{OUT}=5V
- 10μA typical quiescent current
- 1μA typical shutdown mode
- 3.0V to 32V input range
- Stable with small ceramic output capacitors (1μF)
- Over temperature and over current protection
- ±1.5% output voltage tolerance

Applications

- Logic Supply for High Voltage Batteries
- Keep-Alive Supply
- 3-4 Cell Li-ion Batteries Powered systems
- Automotive

Typical Application

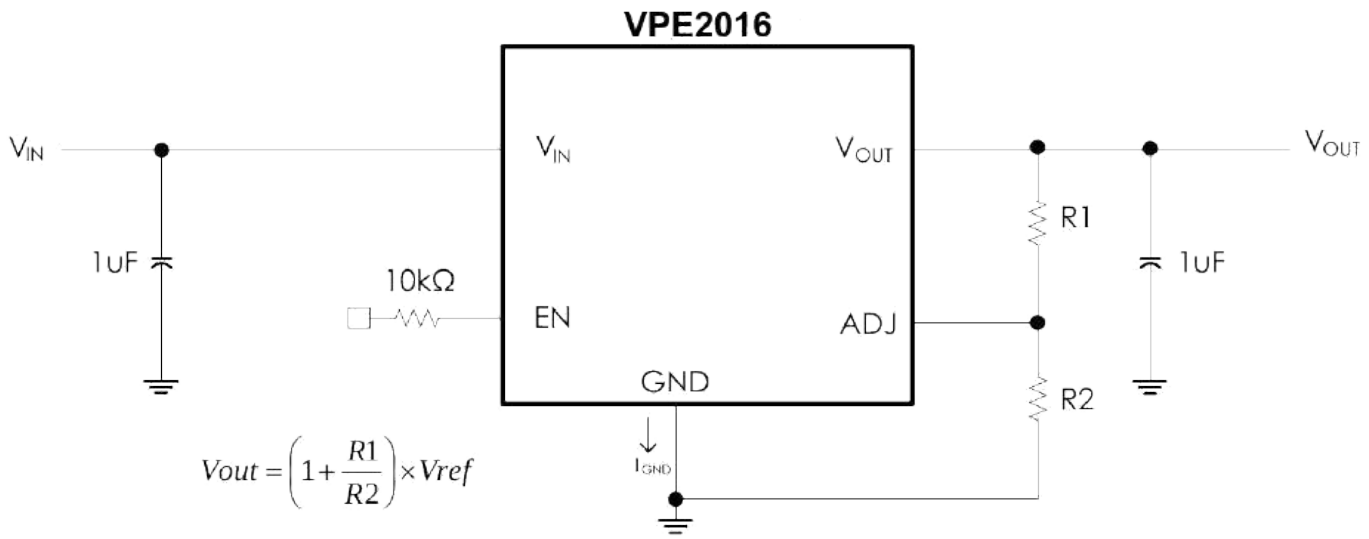
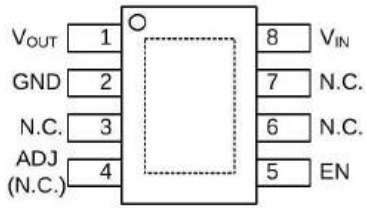


Fig. 1 VPE2016 Typical Application Circuit

Note: R1≥10k is strongly recommended. Especially, Vout was set around Vref

Connection Diagrams



VPE2016-XXSG08VCR

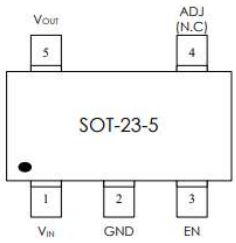
XX Output voltage

SG08 E-SOP-8 Package

VCR RoHS & Halogen free package

Rating: -40 to 125℃

Package in Tape & Reel



VPE2016-XXVN05VCR

XX Output voltage

VN05 SOT-23-5 Package

VCR RoHS & Halogen free package

Rating: -40 to 125℃

Package in Tape & Reel

Order, Mark & Packing Information

Package	Vout	Product ID	Marking	Packing
E-SOP-8L	ADJ	VPE2016-00SG08VCR	2016	Tape & Reel 3kpcs
	3.3V	VPE2016-33SG08VCR		
	5.0V	VPE2016-50SG08VCR		
SOT-23-5L	ADJ	VPE2016-00VN05VCR	2016	Tape & Reel 3Kpcs
	3.3V	VPE2016-33VN05VCR		
	5.0V	VPE2016-50VN05VCR		

Pin Functions

Name	E-SOP 8L	SOT-23-5L	Function
V_{OUT}	1	5	**Output Voltage.**
GND	2	2	**Ground Pin.**
NC	3, 6, 7	N/A	**No connection.**
ADJ (N.C.)	4	4	**Output Voltage Adjust:** Feedback input. Connect to resistive voltage-divider network. R1≥10k is strongly recommended. Especially, Vout was set as Vref. No connect for Fixed Vout.
EN	5	3	**Shutdown Input.** The EN pin is pulled “High” internally. Set the regulator into the disable mode by pulling the EN pin low.
V_{IN}	8	1	**Supply Voltage Input.** Require a minimum input capacitor of close to 1μF to ensure stability and sufficient decoupling from the ground pin.

Functional Block Diagram

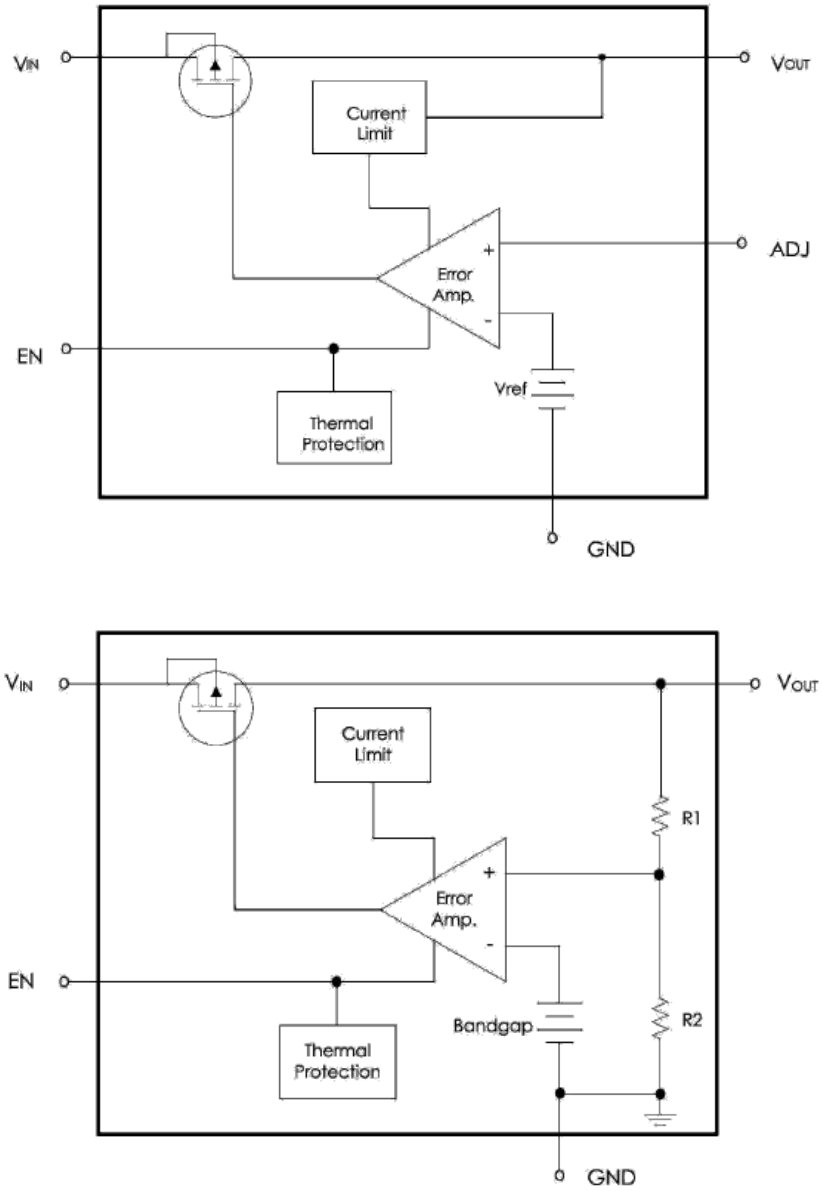


Fig. 2 Functional Block Diagram of VPE2016

Absolute Maximum Ratings

(Notes 1, 2)

V_{IN}, EN ..... –0.3V to 36V
V_{OUT} ..... –0.3V to 8V
Power Dissipation ..... (Note 3)
Storage Temperature Range ..... –65°C to 150°C
Junction Temperature (T_J) ..... 150°C
Lead Temperature (Soldering, 10 sec.) ..... 260°C
ESD Rating (Human Body Model) ..... ±2KV
ESD Rating (Charged Device Model) ..... ±750V
Latch up ..... ±100mA

Operating Ratings

(Notes 1, 2)

Supply Voltage ..... 3.0V to 32V
Operating Temperature Range ..... –40°C to 125°C

Thermal Data

Package	Thermal Resistance	Parameter	Value
E-SOP-8L	θ_{JA} (Note 4)	Junction-to-ambient	50°C/W
	$\theta_{JC(top)}$ (Note 5)	Junction-case (top)	39°C/W
	$\theta_{JC(bottom)}$ (Note 6)	Junction-case (bottom)	10°C/W
SOT-23-5L	θ_{JA} (Note 4)	Junction-to-ambient	152°C/W
	$\theta_{JC(top)}$ (Note 5)	Junction-case (top)	81°C/W

Electrical Characteristics

V_{OUT}(NOM)=5V; unless otherwise specified, all limits guaranteed for V_{IN} = V_{OUT} +1V, EN = 2V, C_{IN} = C_{OUT} = 1μF, T_A=-40°C to 125°C, typical value is T_A=+25°C

Parameter	Symbol	Conditions	Min.	Typ. (Note 7)	Max.	Unit
Reference Voltage	V_{ref}	I_{OUT} = 0.1mA, V_{IN}=$V_{OUT(NOM)}$ +1V ≤ V_{IN} ≤ 36V, T_A= 25°C	1.228	1.24	1.252	V
		I_{OUT} = 0.1mA, V_{IN}=$V_{OUT(NOM)}$ +1V ≤ V_{IN} ≤ 36V, T_A= -40°C ~ 125°C	1.222	1.24	1.258	V
Vref Temperature Coefficient	TC	V_{IN} = V_{OUT} +1V, EN = 2V, I_{OUT} = 0.1mA, Refer to T_A= 25°C	-100	±50	100	ppm/°C
Maximum Output Current	I_{OUT}	Average DC Current Rating	150	-	-	mA
Output Current Limit	I_{LIMIT}	V_{IN} = 12V; Vout=0.9*Vout	180	240	300	mA
Short Circuit Current	I_{Short}	V_{IN} = 12V; V_{OUT} Short to GND	55	75	105	mA
Supply Current	I_Q	I_{OUT} = 0.1mA	-	12	30	μA
		I_{OUT} = 100mA	-	50	100	μA
Shutdown Supply Current	I_Q	V_{OUT} = 0V, EN = GND	-	1.5	5	μA
Dropout Voltage						
	V_{DO}	I_{OUT} = 30mA	-	135	250	mV
		I_{OUT} = 100mA	-	450	900	mV
		I_{OUT} = 150mA	-	780	1500	mV
Line Regulation	ΔV_{OUT}	I_{OUT} = 0.1mA, (V_{OUT} + 1V) ≤ V_{IN} ≤ 36V	-	0.1	0.2	%
Load Regulation	ΔV_{OUT}	0.1mA ≤ I_{OUT} ≤ 100mA	-	0.5	1	%
Output Voltage Noise	e_n	I_{OUT}=10mA, 10Hz ≤ f ≤ 100kHz, V_{OUT} = 5.0V	-	800	-	μV_{RMS}
EN Input Threshold	V_{EN}	V_{IH}, (V_{OUT} + 1V) ≤ V_{IN} ≤ 36V	1.0	-	-	V
		V_{IL}, (V_{OUT} + 1V) ≤ V_{IN} ≤ 36V	-	-	0.3	V
EN Input Bias Current	I_{EN}	EN = GND or V_{IN} (V_{IN}<6V)	-	0.15	0.3	μA
Thermal Shutdown Temperature	T_{SD}	(Note 9)	-	160	-	°C
Thermal Shutdown Hysteresis		(Note 9)	-	30	-	°C
Start-Up Time	t_{ON}	C_{OUT} = 1.0μF, V_{OUT} at 90% of Final Value	-	500	-	μs

- **Note 1:** Absolute Maximum ratings indicate limits beyond which damage may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions.
- **Note 2:** All voltages are with respect to the potential at the ground pin.
- **Note 3:** Maximum Power dissipation for the device is calculated using the following equations:

$$P_D = (T_{J(MAX)} - T_A) / \theta_{JA}$$

  Where T_J(MAX) is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance. E.g. for the E-SOP-8 package θ_{JA} = 50°C/W, T_J (MAX) = 150°C and using T_A = 25°C, the maximum power dissipation is found to be 2.5W. The derating factor ($-1/\theta_{JA}$) = -20mW/°C, thus below 25°C the power dissipation figure can be increased by 20mW per degree, and similarity decreased by this factor for temperatures above 25°C.
- **Note 4:** θ_{JA} is simulated in the natural convection at T_A=25°C on a highly effective thermal conductivity (thermal land area completed with $>$3x3cm^2 area) board (2 layers, 2S0P) according to the JEDEC 51-7 thermal measurement standard.
- **Note 5:** $\theta_{JC(top)}$ represents the heat resistance between the chip junction and the top surface of package.
- **Note 6:** $\theta_{JC(bottom)}$ represents the heat resistance between the chip junction and the center of the exposed pad on the underside of the package.
- **Note 7:** Typical Values represent the most likely parametric norm.
- **Note 8:** Dropout voltage is measured by reducing V_{IN} until V_{OUT} drops to 98% its nominal value.
- **Note 9:** Design Guarantee.

Typical Performance Characteristics

Unless otherwise specified, V_{IN} = $V_{OUT(NOM)}$ + 1V, V_{OUT}=5V, C_{IN} = C_{OUT} = 1.0μF, T_A = 25°C, EN = 2V

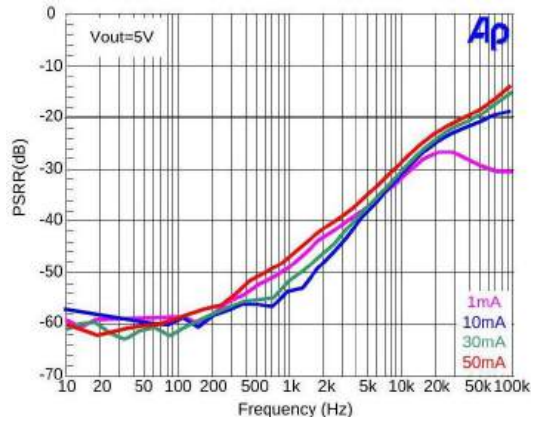


Figure 2. PSRR vs. Frequency (V_{IN}=6V, V_{OUT}=5V)

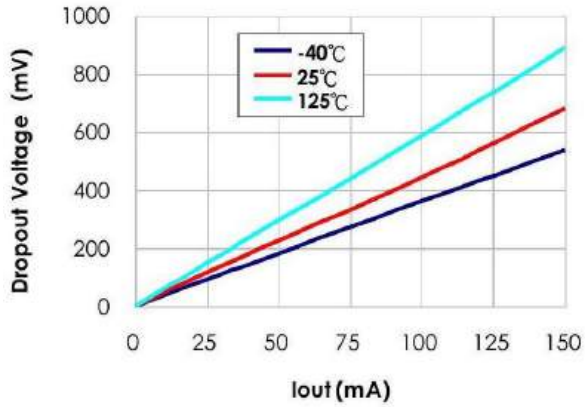


Figure 3. Dropout Voltage vs. Load Current (V_{OUT}=5.0V)

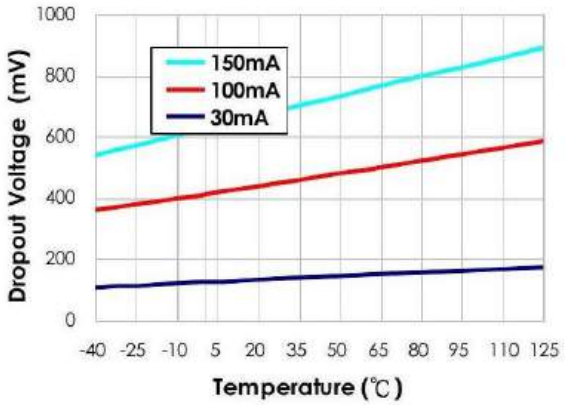


Figure 4. Dropout Voltage vs. Temp (V_{OUT}=5.0V)

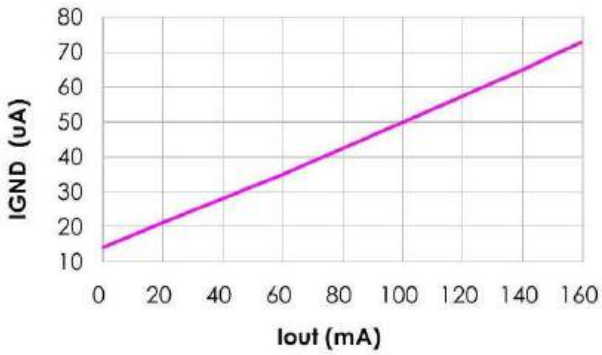


Figure 5. Ground Current vs. I_{OUT} (V_{OUT}=5.0V, T_A=25°C)

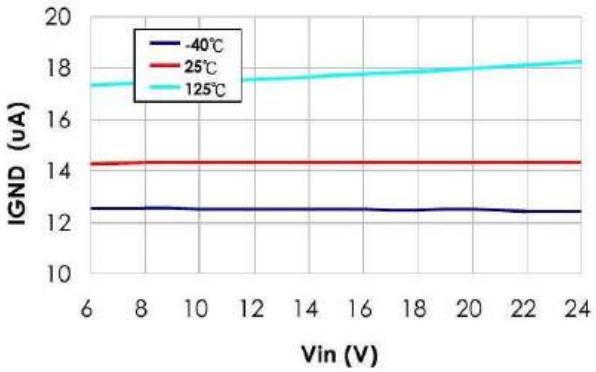


Figure 6. Ground Current vs. V_{IN} (V_{OUT}=5.0V)

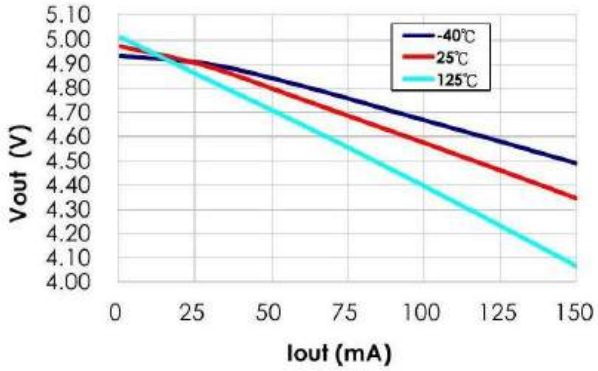


Figure 7. V_{OUT} vs. I_{OUT} (V_{OUT}=5.0V)

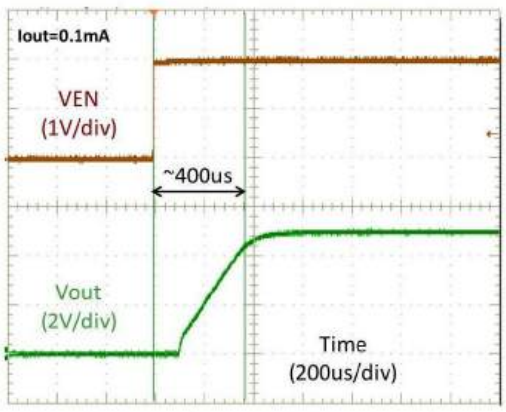


Figure 8. Enable Response (V_{OUT}=5.0V, I_{OUT}=0.1mA)

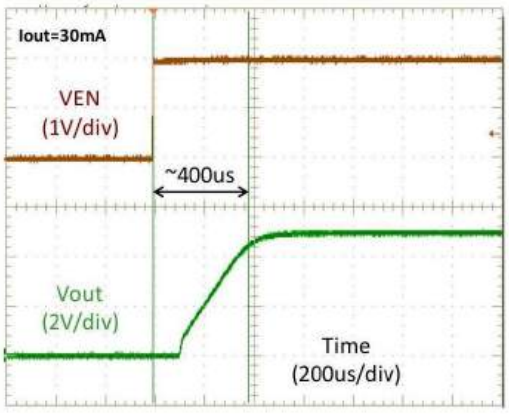


Figure 9. Enable Response (V_{OUT}=5.0V, I_{OUT}=30mA)

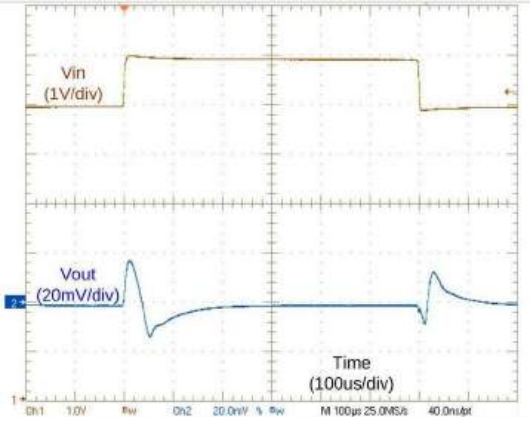


Figure 10. Line Transient (I_{OUT}=1mA)

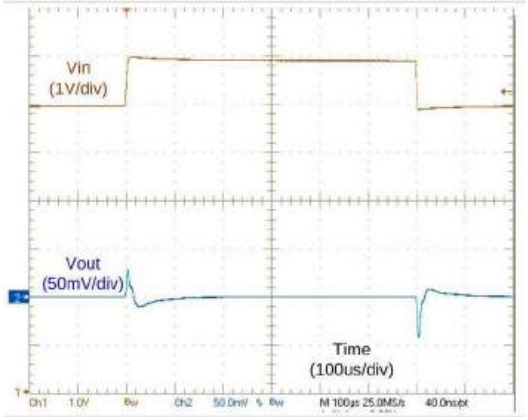


Figure 11. Line Transient (I_{OUT}=30mA)

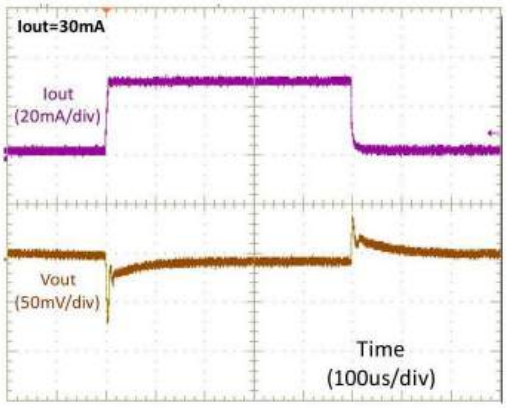


Figure 12. Load Transient (V_{OUT}=5.0V)

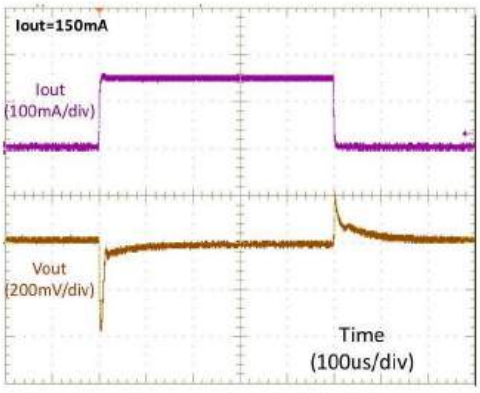


Figure 13. Load Transient (V_{OUT}=5.0V)

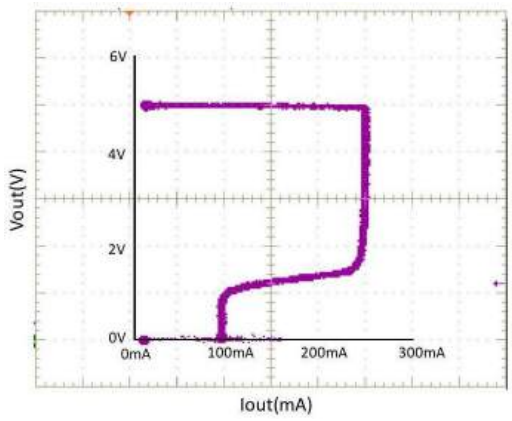


Figure 14. Current Limit V_{IN}=12V (Note 10)

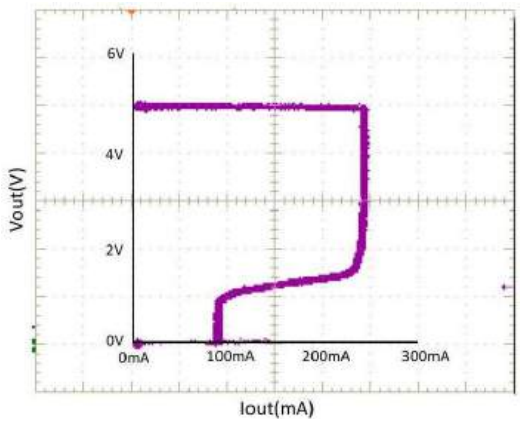


Figure 15. Current Limit V_{IN}=24V (Note 10)

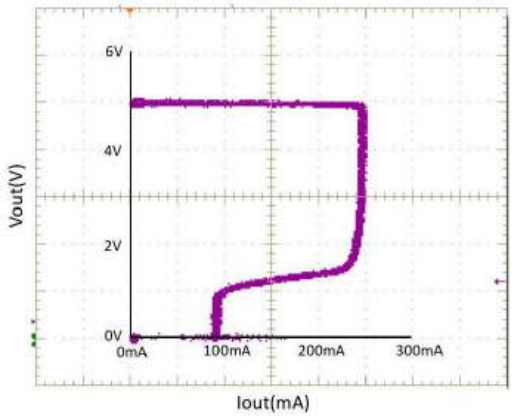


Figure 16. Current Limit V_{IN}=36V (Note 10)

Note 10: The Foldback current limit waveform is tested by enabling on VPE2016 with Cout=1000uF.

Application Information

General Description

Referring to Fig.2 as shown in the Functional Block Diagram section, the VPE2016 adopts the classical regulator topology in which negative feedback control is used to perform the desired voltage regulating function. The negative feedback is formed by using feedback resistors (R1, R2) to sample the output voltage for the non-inverting input of the error amplifier, whose inverting input is set to the bandgap reference voltage. By the virtue of its high open-loop gain, the error amplifier operates to ensure that the sampled output feedback voltage at its non-inverting input is virtually equal to the preset bandgap reference voltage.

The error amplifier compares the voltage difference at its inputs and produces an appropriate driving voltage to the P-channel MOS pass transistor to control the amount of current reaching the output. If there are changes in the output voltage due to load changes, the feedback resistors register such changes to the non-inverting input of the error amplifier. The error amplifier then adjusts its driving voltage to maintain virtual short between its two input nodes under all loading conditions. In a nutshell, the regulation of the output voltage is achieved as a direct result of the error amplifier keeping its input voltages equal. This negative feedback control topology is further augmented by the shutdown, the fault detection, and the temperature and current protection circuitry. With sensing output voltage, the current limit level would be Foldback to lower level during Vout shorted to GND.

Output Capacitor

The VPE2016 is specially designed for use with ceramic output capacitors of as low as 1.0μF to take advantage of the savings in cost and space as well as the superior filtering of high frequency noise. Capacitors of higher value or other types may be used, but it is important to make sure its equivalent series resistance (ESR) is restricted to less than 0.5Ω. The use of larger capacitors with smaller ESR values is desirable for applications involving large and fast input or output transients, as well as for situations where the application systems are not physically located immediately adjacent to the battery power source. Typical ceramic capacitors suitable for use with the VPE2016 are X5R and X7R. The X5R and the X7R capacitors are able to maintain their capacitance values to within ±20% and ±10%, respectively, as the temperature increases.

No-Load Stability

The VPE2016 is capable of stable operation during no-load conditions, a mandatory feature for some applications such as CMOS RAM keep-alive operations.

Input Capacitor

A minimum input capacitance of 1μF is required for VPE2016. The capacitor value may be increased without limit. Improper workbench set-ups may have adverse effects on the normal operation of the regulator. A case in point is the instability that may result from long supply lead inductance coupling to the output through the gate capacitance of the pass transistor. This will establish a pseudo LCR network, and is likely to happen under high current conditions or near dropout. A 10μF tantalum input capacitor will dampen the parasitic LCR action thanks to its high ESR. However, cautions should be exercised to avoid regulator short-circuit damage when tantalum capacitors are used, for they are prone to fail in short-circuit operating conditions.

Power Dissipation and Thermal Shutdown

Thermal overload results from excessive power dissipation that causes the IC junction temperature to increase beyond a safe operating level. The VPE2016 relies on dedicated thermal shutdown circuitry to limit its total power dissipation. An IC junction temperature T_J exceeding 150°C will trigger the thermal shutdown logic, turning off the P-channel MOS pass transistor. The pass transistor turns on again after the junction cools off by about 30°C. When continuous thermal overload conditions persist, this thermal shutdown action then results in a pulsed waveform at the output of the regulator.

The concept of thermal resistance θ_{JA} (°C/W) is often used to describe an IC junction's relative readiness in allowing its thermal energy to dissipate to its ambient air. An IC junction with a low thermal resistance is preferred because it is relatively effective in dissipating its thermal energy to its ambient, thus resulting in a relatively low and desirable junction temperature. The relationship between θ_{JA} and T_J is as follows:

$$T_J = \theta_{JA}(P_D) + T_A \quad \text{(Eq. 1)}$$

T_A is the ambient temperature, and P_D is the power generated by the IC and can be written as:

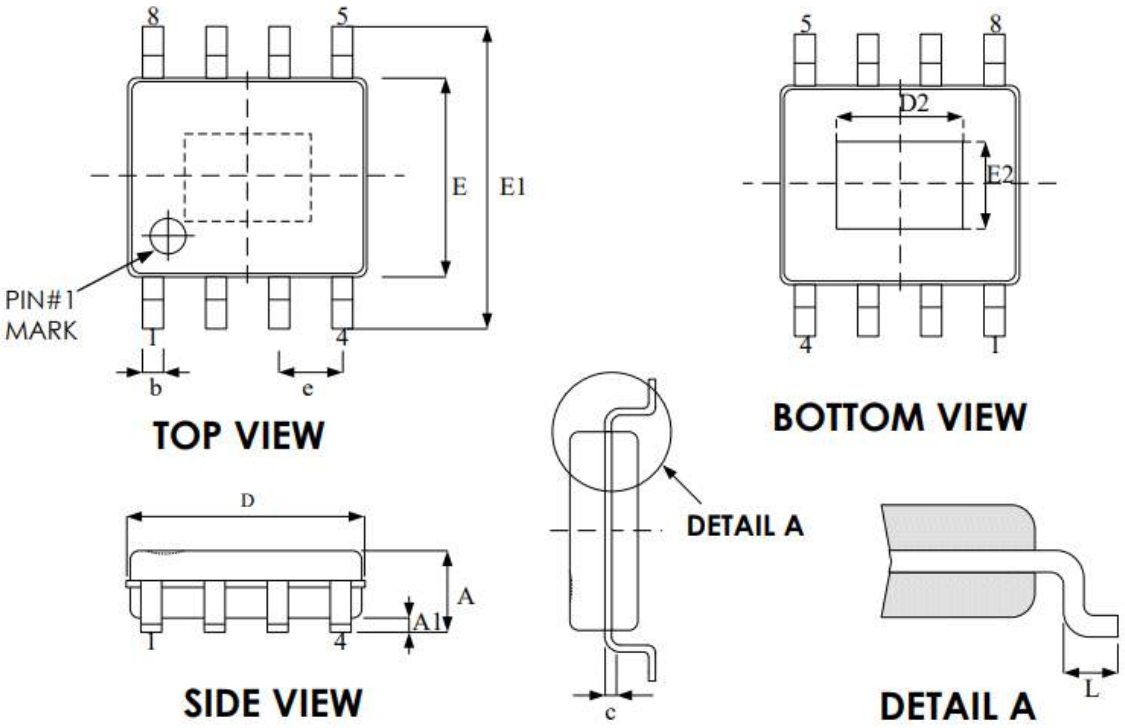
$$P_D = I_{OUT}(V_{IN} - V_{OUT}) \quad \text{(Eq. 2)}$$

As the above equations show, it is desirable to work with ICs whose θ_{JA} values are small such that T_J does not increase strongly with P_D. To avoid thermally overloading the VPE2016, refrain from exceeding the absolute maximum junction temperature rating of 150°C under continuous operating conditions. Overstressing the regulator with high loading currents and elevated input-to-output differential voltages can increase the IC die temperature significantly.

Shutdown

The VPE2016 enters the sleep mode when the EN pin is low. When this occurs, the pass transistor, the error amplifier, and the biasing circuits, including the bandgap reference, are turned off, thus reducing the supply current to typically 1μA. Such a low supply current makes the VPE2016 best suited for battery-powered applications. The maximum guaranteed voltage at the EN pin for the sleep mode to take effect is 0.3V. The EN pin is pulled high internally.

Package Outline Drawing (E-SOP-8L)



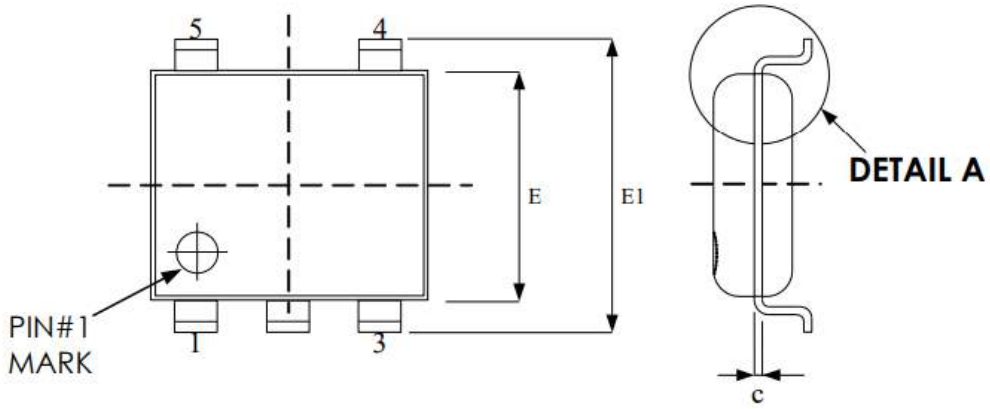
Symbol	Dimension in mm	
	Min.	Max.
A	1.35	1.75
A1	0.00	0.25
b	0.31	0.51
c	0.10	0.25
D	4.80	5.00
E	3.81	4.00
E1	5.79	6.20
e	1.27 BSC	
L	0.40	1.27

Exposed Pad

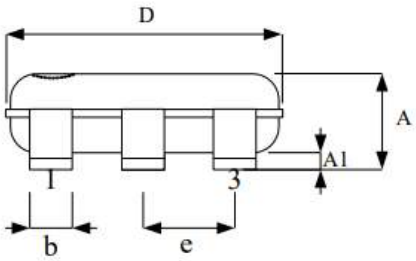
Symbol	Dimension in mm	
	Min.	Max.
D2	2.80	3.50
E2	2.00	2.60

All dimensions are in millimeters.

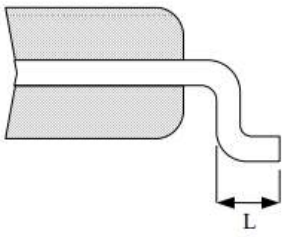
Package Outline Drawing (SOT-23-5L)



TOP VIEW



SIDE VIEW



DETAIL A

Symbol	Dimension in mm	
	Min.	Max.
A	0.90	1.45
A1	0.00	0.15
b	0.30	0.50
c	0.08	0.25
D	2.70	3.10
E	1.40	1.80
E1	2.60	3.00
e	0.95 BSC	
L	0.30	0.60

All dimensions are in millimeters.

Disclaimer

The information provided in this datasheet is believed to be accurate and reliable. Errors or omissions are expected. indiaVP Semiconductor Pvt. Ltd. reserves the right to make changes to the product specifications without prior notice. Users should verify the suitability of the product for their specific applications. Please visit our website for the latest datasheet.

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