Description

The VPE2014 is a high voltage, low quiescent current, low dropout regulator with 150mA output driving capacity. The VPE2014, which operates over an input range up to 40V, is stable with any capacitors, whose capacitance is larger than 1μF, and suitable for powering battery-management ICs because of the virtue of its low quiescent current consumption and low dropout voltage. Below the maximum power dissipation (please refer to Note 5), it guarantees delivery of 100mA output current, and supports preset output voltages ranging from 1.3V to 6.0V with 0.1V increment.

VPE2014 features also include bandgap voltage reference, constant current limiting and thermal overload protection. Both miniature SOT-23-5 and SOT-89-3 package options are offered to provide flexibility for different applications.

Key Features

- 150mA output current driving capacity
- 780mV typical dropout at Io=150mA
- 12μA typical quiescent current
- 1μA typical shutdown mode
- Up to 40V input range
- Stable with small ceramic output capacitors (1μF)
- Over temperature and over current protection

Applications

- Logic Supply for High Voltage Batteries
- Keep-Alive Supply
- 3-4 Cell Li-ion Batteries Powered systems

Typical Application

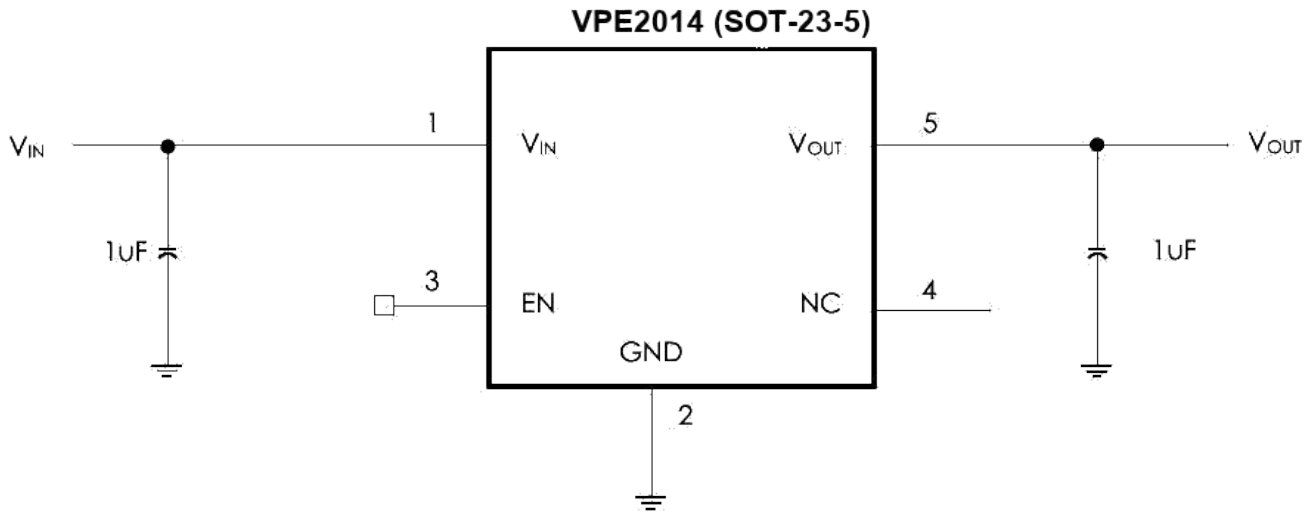
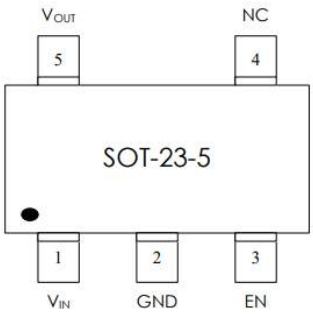


Fig. 1 VPE2014 (SOT-23-5) Typical Application Circuit

Connection Diagrams

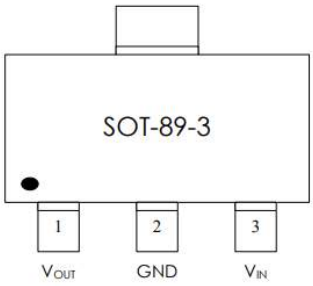


VPE2014-XXVF05NRR

XX Output voltage

VF05 SOT-23-5 Package

NRR RoHS & Halogen free package
Rating: -40 to 85℃
Package in Tape & Reel



VPE2014-XXVG03NRR

XX Output voltage

VG03 SOT-89-3 Package

NRR RoHS & Halogen free package
Rating: -40 to 85℃
Package in Tape & Reel

Order, Mark & Packing Information

Package	Vout	Product ID	Marking	Packing
SOT-23-5	3.0V	VPE2014-30VF05NRR	2014	Tape & Reel 3Kpcs
	3.3V	VPE2014-33VF05NRR		
	5.0V	VPE2014-50VF05NRR		
SOT-89-3	3.0V	VPE2014-30VG03NRR	2014	Tape & Reel 1Kpcs
	3.3V	VPE2014-33VG03NRR		
	5.0V	VPE2014-50VG03NRR		

Pin Functions

Name	SOT-23-5	SOT-89-3	Function
V_{IN}	1	3	**Supply Voltage Input.** Require a minimum input capacitor of close to 1μF to ensure stability and sufficient decoupling from the ground pin.
GND	2	2	**Ground Pin.**
EN	3	N/A	**Shutdown Input.** The EN pin is pulled “High” internally. Set the regulator into the disable mode by pulling the EN pin low.
NC	4	N/A	**No connection.**
V_{OUT}	5	1	**Output Voltage.**

Functional Block Diagram

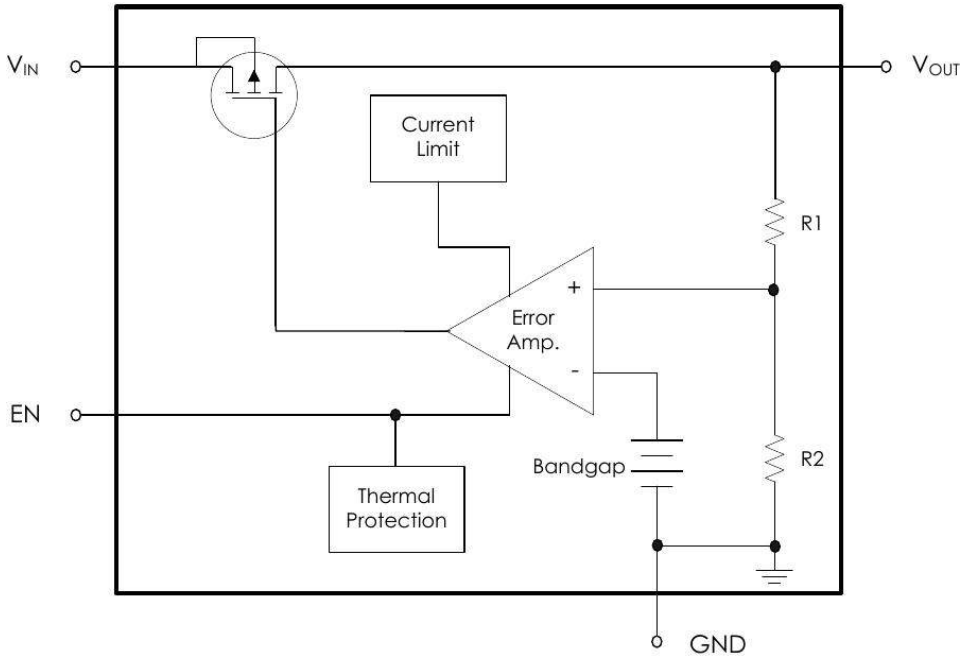


Fig. 2 Functional Block Diagram of VPE2014

Absolute Maximum Ratings

(Notes 1, 2)

V_{IN}, EN ..... –0.3V to 42V
V_{OUT} ..... –0.3V to 13.2V
Power Dissipation ..... (Note 3)
Storage Temperature Range ..... –65°C to 150°C
Junction Temperature (T_J) ..... 160°C
Lead Temperature (Soldering, 10 sec.) ..... 260°C
ESD Rating (Human Body Model) 2KV

Operating Ratings

(Notes 1, 2)

Supply Voltage ..... 2.7V to 40V
Operating Temperature Range ..... –40°C to 85°C
Thermal Resistance (θ_{JA}, Note 3) ... 152°C/W (SOT-23-5)
90°C/W (SOT-89-3)
Thermal Resistance (θ_{JC}, Note 4) .... 81°C/W (SOT-23-5)
52°C/W (SOT-89-3)

Electrical Characteristics

T_A=25°C, V_{OUT}(NOM)=5V; unless otherwise specified, all limits guaranteed for V_{IN} = V_{OUT} +1V, C_{IN} = C_{OUT} = 1μF.

Parameter	Symbol	Conditions	Min.	Typ. (Note 6)	Max.	Unit
Output Voltage Tolerance	ΔV_{OTL}	I_{OUT} = 10mA, $V_{OUT(NOM)}$ +1V ≤ V_{IN} ≤ 40V	-1	-	+1	% of $V_{OUT(NOM)}$
Maximum Output Current	I_{OUT}	Average DC Current Rating	150	-	-	mA
Output Current Limit	I_{LIMIT}	-	300	-	-	mA
Supply Current	I_Q	I_{OUT} = 0.1mA	-	12	30	μA
		I_{OUT} = 100mA	-	50	100	μA
		I_{OUT} = 150mA	-	80	130	μA
Shutdown Supply Current	I_Q	V_{OUT} = 0V, EN = GND	-	1	5	μA
Dropout Voltage						
	V_{DO}	I_{OUT} = 30mA	-	135	-	mV
		I_{OUT} = 100mA	-	500	-	mV
		I_{OUT} = 150mA	-	780	-	mV
Line Regulation	ΔV_{OUT}	I_{OUT} = 1mA, (V_{OUT} + 1V) ≤ V_{IN} ≤ 40V	-	0.1	-	%
Load Regulation	ΔV_{OUT}	0.1mA ≤ I_{OUT} ≤ 100mA	-	0.5	-	%
Output Voltage Noise	e_n	I_{OUT}=10mA, 10Hz ≤ f ≤ 100kHz, V_{OUT} = 5.0V	-	800	-	μV_{RMS}
EN Input Threshold	V_{EN}	V_{IH}, (V_{OUT} + 1V) ≤ V_{IN} ≤ 40V	1.0	-	-	V
		V_{IL}, (V_{OUT} + 1V) ≤ V_{IN} ≤ 40V	-	-	0.3	V
EN Input Bias Current	I_{EN}	EN = GND or V_{IN}	-	0.1	-	μA
Thermal Shutdown Temperature	T_{SD}	-	-	160	-	°C
Thermal Shutdown Hysteresis		-	-	30	-	°C
Start-Up Time	t_{ON}	C_{OUT} = 1.0μF, V_{OUT} at 90% of Final Value	-	500	-	μs

- **Note 1:** Absolute maximum ratings indicate limits beyond which damage may occur.
- **Note 2:** All voltages are in respect to the potential of the ground pin.
- **Note 3:** θ_{JA} is measured in the natural convection at T_A=25°C on a high effectively thermal conductivity test board (2 layers, 2S0P).
- **Note 4:** θ_{JC} represents the resistance between the chip and the top of the package case.
- **Note 5:** Maximum power dissipation for the device is calculated using the following equation:

$$P_D = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

Where T_J(MAX) is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance. For example, for the SOT-89-3 package θ_{JA}=90°C/W, T_J(MAX)=160°C and using T_A=25°C, the maximum power dissipation is 1.5W. The derating factor (-1/θ_{JA})=-11.1mW/°C. Below 25°C the power dissipation figure can be increased by 11.1mW per degree and similarly decreased by this factor for temperatures above 25°C.

- **Note 6:** Typical values represent the most likely parametric norm.
- **Note 7:** Dropout voltage is measured by reducing V_{IN} until V_{OUT} drops to 98% its nominal value.

Typical Performance Characteristics

Unless otherwise specified, V_{IN} = $V_{OUT(NOM)}$ + 1V, V_{OUT}=5V, C_{IN} = C_{OUT} = 1.0μF, T_A = 25°C, EN = 2V

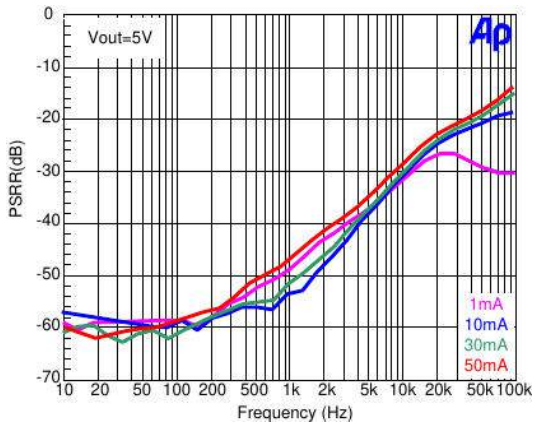


Figure 3. PSRR vs. Frequency (V_{OUT}=5.0V)

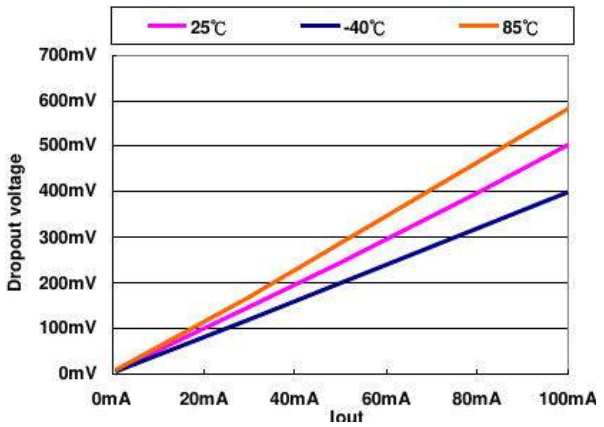


Figure 4. Dropout Voltage vs. Load Current (V_{OUT}=5.0V)

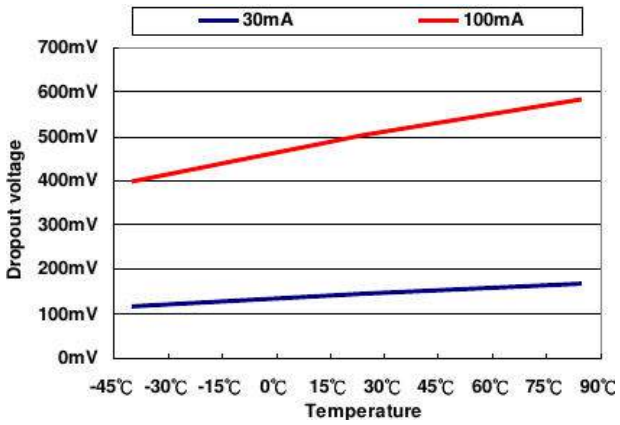


Figure 5. Dropout Voltage vs. Temp (V_{OUT}=5.0V)

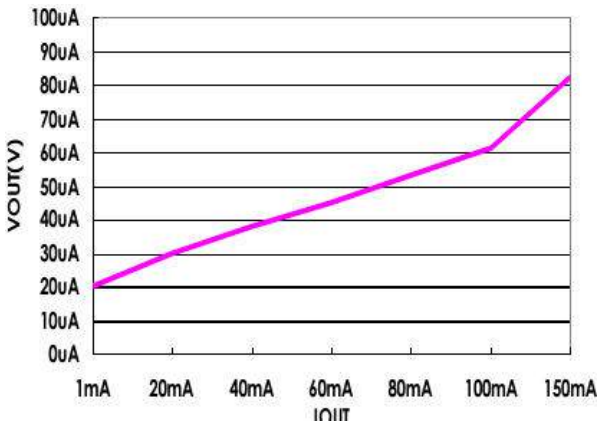


Figure 6. Ground Current vs. I_{OUT} (V_{OUT}=3.3V, T_A=25°C)

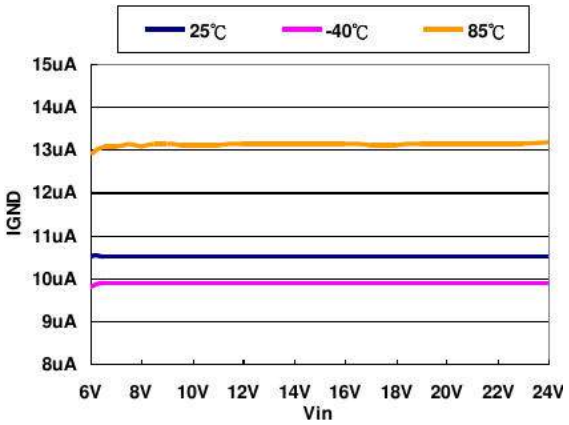


Figure 7. Ground Current vs. V_{IN} (V_{OUT}=5.0V)

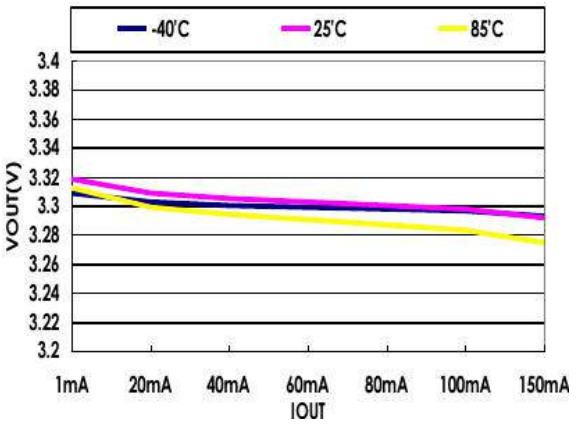


Figure 8. V_{OUT} vs. I_{OUT} (V_{OUT}=3.3V)

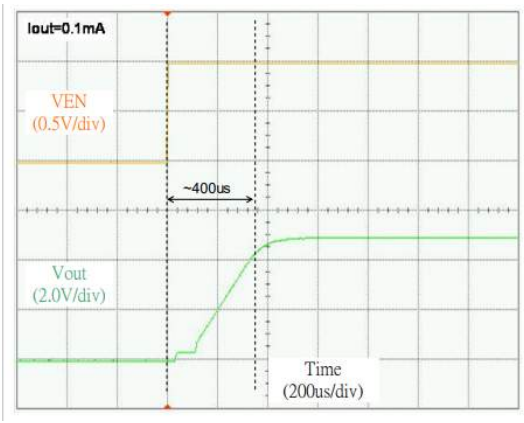


Figure 9. Enable Response (V_{OUT}=5.0V, I_{OUT}=0.1mA)

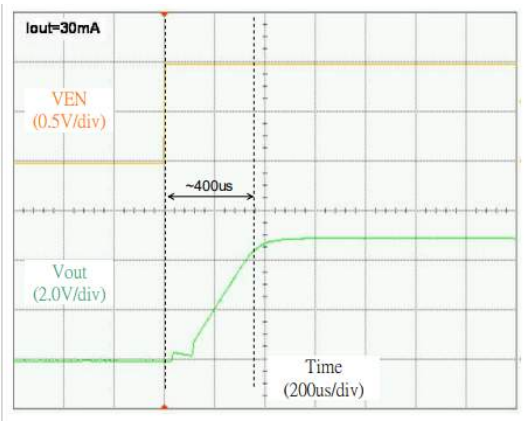


Figure 10. Enable Response (V_{OUT}=5.0V, I_{OUT}=30mA)

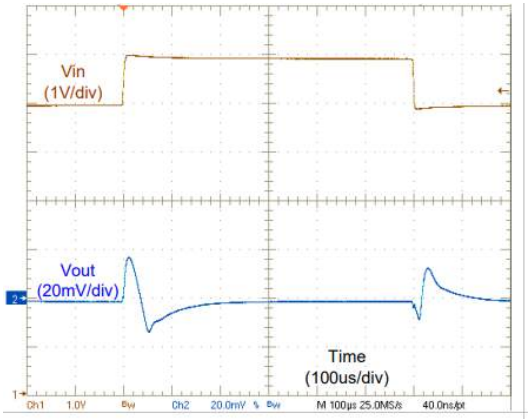


Figure 11. Line Transient (I_{OUT}=1mA)

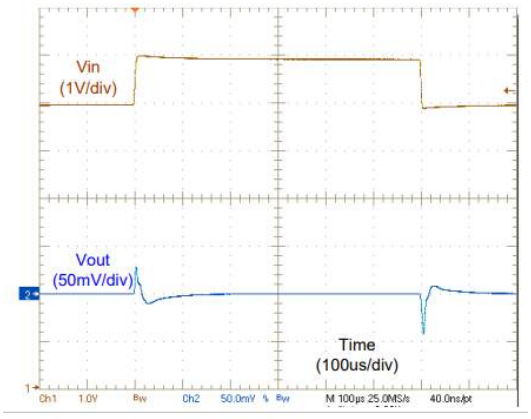


Figure 12. Line Transient (I_{OUT}=30mA)

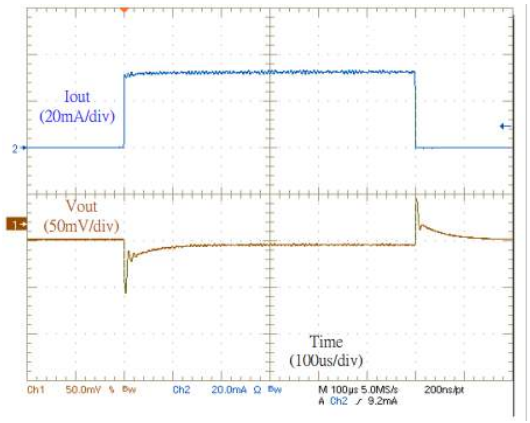


Figure 13. Load Transient (V_{OUT}=5.0V)

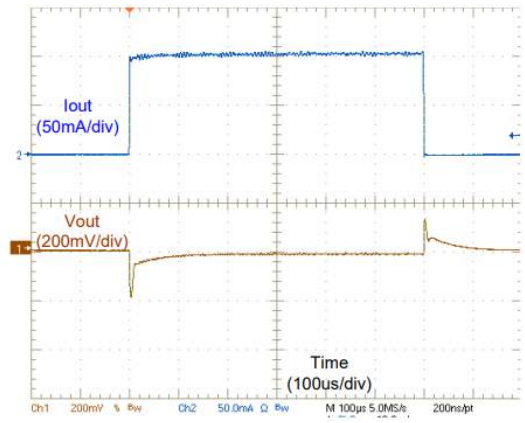


Figure 14. Load Transient (V_{OUT}=5.0V)

Application Information

General Description

Referring to Fig.2 as shown in the Functional Block Diagram section, the VPE2014 adopts the classical regulator topology in which negative feedback control is used to perform the desired voltage regulating function. The negative feedback is formed by using feedback resistors (R1, R2) to sample the output voltage for the non-inverting input of the error amplifier, whose inverting input is set to the bandgap reference voltage. By the virtue of its high open-loop gain, the error amplifier operates to ensure that the sampled output feedback voltage at its non-inverting input is virtually equal to the preset bandgap reference voltage.

The error amplifier compares the voltage difference at its inputs and produces an appropriate driving voltage to the P-channel MOS pass transistor to control the amount of current reaching the output. If there are changes in the output voltage due to load changes, the feedback resistors register such changes to the non-inverting input of the error amplifier. The error amplifier then adjusts its driving voltage to maintain virtual short between its two input nodes under all loading conditions. In a nutshell, the regulation of the output voltage is achieved as a direct result of the error amplifier keeping its input voltages equal. This negative feedback control topology is further augmented by the shutdown, the fault detection, and the temperature and current protection circuitry.

Output Capacitor

The VPE2014 is specially designed for use with ceramic output capacitors of as low as 1.0μF to take advantage of the savings in cost and space as well as the superior filtering of high frequency noise. Capacitors of higher value or other types may be used, but it is important to make sure its equivalent series resistance (ESR) is restricted to less than 0.5Ω. The use of larger capacitors with smaller ESR values is desirable for applications involving large and fast input or output transients, as well as for situations where the application systems are not physically located immediately adjacent to the battery power source. Typical ceramic capacitors suitable for use with the VPE2014 are X5R and X7R. The X5R and the X7R capacitors are able to maintain their capacitance values to within ±20% and ±10%, respectively, as the temperature increases.

No-Load Stability

The VPE2014 is capable of stable operation during no-load conditions, a mandatory feature for some applications such as CMOS RAM keep-alive operations.

Input Capacitor

A minimum input capacitance of 1μF is required for VPE2014. The capacitor value may be increased without limit. Improper workbench set-ups may have adverse effects on the normal operation of the regulator. A case in point is the instability that may result from long supply lead inductance coupling to the output through the gate capacitance of the pass transistor. This will establish a pseudo LCR network, and is likely to happen under high current conditions or near dropout. A 10μF tantalum input capacitor will dampen the parasitic LCR action thanks to its high ESR. However, cautions should be exercised to avoid regulator short-circuit damage when tantalum capacitors are used, for they are prone to fail in short-circuit operating conditions.

Power Dissipation and Thermal Shutdown

Thermal overload results from excessive power dissipation that causes the IC junction temperature to increase beyond a safe operating level. The VPE2014 relies on dedicated thermal shutdown circuitry to limit its total power dissipation. An IC junction temperature T_J exceeding 160°C will trigger the thermal shutdown logic, turning off the P-channel MOS pass transistor. The pass transistor turns on again after the junction cools off by about 30°C. When continuous thermal overload conditions persist, this thermal shutdown action then results in a pulsed waveform at the output of the regulator.

The concept of thermal resistance θ_{JA} (°C/W) is often used to describe an IC junction's relative readiness in allowing its thermal energy to dissipate to its ambient air. An IC junction with a low thermal resistance is preferred because it is relatively effective in dissipating its thermal energy to its ambient, thus resulting in a relatively low and desirable junction temperature. The relationship between θ_{JA} and T_J is as follows:

$$T_J = \theta_{JA}(P_D) + T_A \quad \text{(Eq. 1)}$$

T_A is the ambient temperature, and P_D is the power generated by the IC and can be written as:

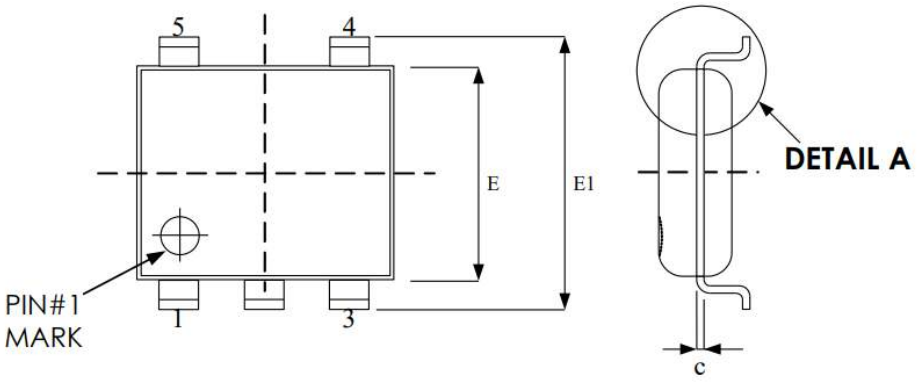
$$P_D = I_{OUT}(V_{IN} - V_{OUT}) \quad \text{(Eq. 2)}$$

As the above equations show, it is desirable to work with ICs whose θ_{JA} values are small such that T_J does not increase strongly with P_D. To avoid thermally overloading the VPE2014, refrain from exceeding the absolute maximum junction temperature rating of 160°C under continuous operating conditions. Overstressing the regulator with high loading currents and elevated input-to-output differential voltages can increase the IC die temperature significantly.

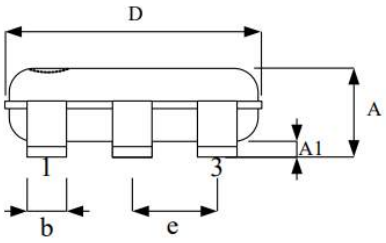
Shutdown

The VPE2014 enters the sleep mode when the EN pin is low. When this occurs, the pass transistor, the error amplifier, and the biasing circuits, including the bandgap reference, are turned off, thus reducing the supply current to typically 1μA. Such a low supply current makes the VPE2014 best suited for battery-powered applications. The maximum guaranteed voltage at the EN pin for the sleep mode to take effect is 0.3V. The EN pin is pulled high internally.

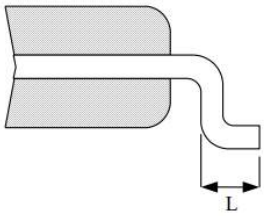
Package Outline Drawing(SOT-23-5)



TOP VIEW



SIDE VIEW

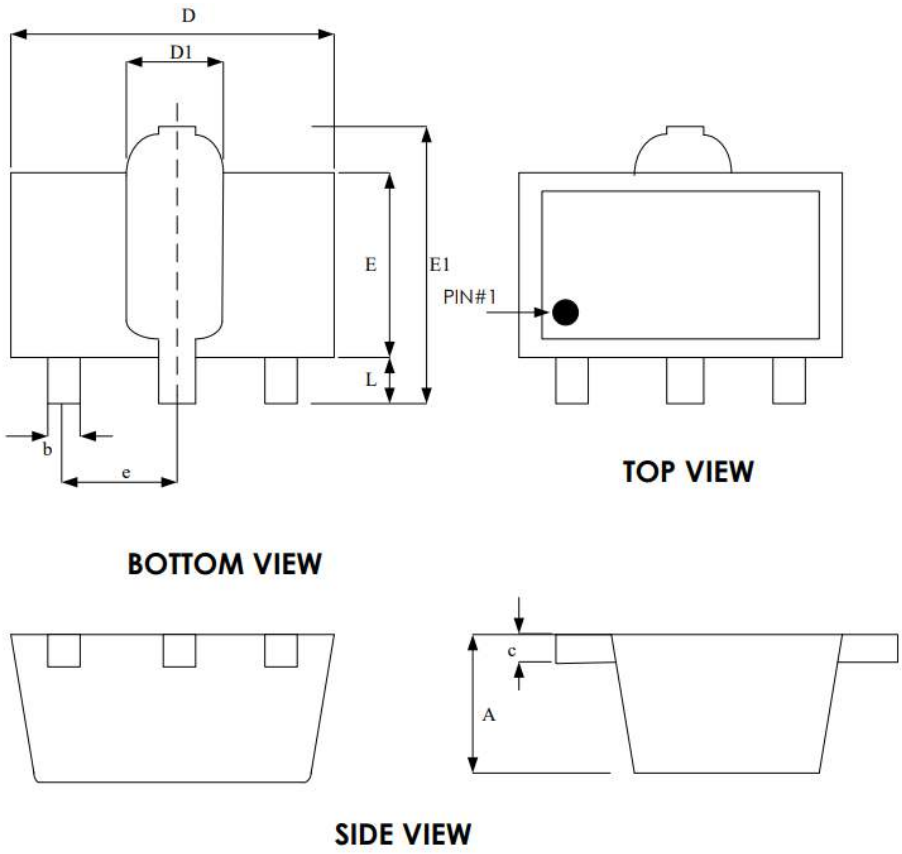


DETAIL A

Symbol	Dimension in mm	
	Min.	Max.
A	0.90	1.45
A1	0.00	0.15
b	0.30	0.50
c	0.08	0.25
D	2.70	3.10
E	1.40	1.80
E1	2.60	3.00
e	0.95 BSC	
L	0.30	0.60

All dimensions are in millimeters.

Package Outline Drawing (SOT-89-3)



Symbol	Dimension in mm	
	Min.	Max.
A	1.40	1.60
b	0.40	0.56
c	0.35	0.41
D	4.40	4.60
D1	1.50	1.83
E	2.29	2.60
E1	3.94	4.25
e	1.50 BSC	
L	0.89	1.20

All dimensions are in millimeters.

Disclaimer

The information provided in this datasheet is believed to be accurate and reliable. Errors or omissions are expected. indiaVP Semiconductor Pvt. Ltd. reserves the right to make changes to the product specifications without prior notice. Users should verify the suitability of the product for their specific applications. Please visit our website for the latest datasheet.

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