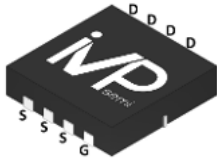
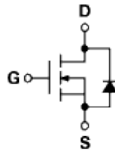


PDFN3.3*3.3

Symbol


Parameter	Value	Unit
V_{DS}	80	V
$R_{DS(ON)-Max}$	8.5	m Ω
I_D	51	A

Key Features

- Advanced trench cell design
- Reliable and Rugged
- ROHS Compliant & Halogen-Free
- 100% UIS and Rg Tested

Applications

- Motor drivers
- DC-DC Converter

Ordering Information

Ordering part Number	Marking code	Package	Form
VPLMDF7140	7140	PDFN3.3*3.3	Tape & Reel

Absolute Maximum Ratings ($T_j = 25^\circ\text{C}$, unless otherwise specified)

Parameter	Symbol	Rating	Unit	
Drain-Source Voltage	V_{DS}	80	V	
Gate-Source Voltage	V_{GS}	± 20	V	
Maximum Junction Temperature	T_J	150	$^\circ\text{C}$	
Storage Temperature Range	T_{STG}	-55 to 150	$^\circ\text{C}$	
Diode Continuous Forward Current	I_S	18	A	
Pulse Drain Current Tested	$I_{DM}^{(1)}$	127	A	
Continuous Drain Current	I_D	$T_C=25^\circ\text{C}$	51	A
		$T_C=100^\circ\text{C}$	32	A
Maximum Power Dissipation	P_D	$T_C=25^\circ\text{C}$	36	W
		$T_C=100^\circ\text{C}$	14	W
Continuous Drain Current	I_D	$T_A=25^\circ\text{C}$	10.9	A
		$T_A=70^\circ\text{C}$	8.7	A
Maximum Power Dissipation	P_D	$T_A=25^\circ\text{C}$	1.7	W
		$T_A=70^\circ\text{C}$	1.1	W
Avalanche Current, Single pulse	$I_{AS}^{(2)}$	L=0.1mH	28	A
		L=0.5mH	16	A
Avalanche Energy, Single pulse	$E_{AS}^{(2)}$	L=0.1mH	39	mJ
		L=0.5mH	64	mJ

Thermal Characteristics

Parameter	Symbol	Rating	Unit
Thermal Resistance-Junction to Case	$R_{\theta JC}$	3.5	$^\circ\text{C/W}$
Thermal Resistance-Junction to Ambient	$R_{\theta JA}^{(3)}$	75	$^\circ\text{C/W}$

- (1) Max. current is limited by Junction temperature.
- (2) UIS tested and pulse width are limited by maximum junction temperature 150°C
- (3) Surface Mounted on 1in^2 FR-4 board with 1oz.

Electrical Characteristics ($T_j = 25^\circ\text{C}$, unless otherwise specified)

Static Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	80	-	-	V	$V_{GS}=0V, I_{DS}=250\mu A$
Zero Gate Voltage Drain Current	I_{DSS}	-	-	1	μA	$V_{DS}=64V, V_{GS}=0V$
Gate Threshold Voltage	$V_{GS(th)}$	2	3	4	V	$V_{DS}=V_{GS}, I_{DS}=250\mu A$
Gate Leakage Current	I_{GSS}	-	-	± 100	nA	$V_{GS}=\pm 20V, V_{DS}=0V$
Drain-Source On-state Resistance	$R_{DS(ON)}^{(4)}$	-	7	8.5	m Ω	$V_{GS}=10V, I_{DS}=20A$
Forward Transconductance	g_{fs}	-	18	-	S	$V_{DS}=5V, I_{DS}=10A$

Dynamic Characteristics⁽⁵⁾

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Gate Resistance	R_G	-	1	-	Ω	$V_{GS}=0V, V_{DS}=0V,$ Freq.=1MHz
Input Capacitance	C_{iss}	-	1583	-	pF	$V_{GS}=0V, V_{DS}=40V,$ Freq.=1MHz
Output Capacitance	C_{oss}	-	497	-		
Reverse Transfer Capacitance	C_{rss}	-	48	-		
Turn-on Delay Time	$t_{d(ON)}$	-	13	-	nS	$V_{GS}=10V, V_{DS}=40V,$ $I_D=1A, R_{GEN}=1\Omega$
Turn-on Rise Time	t_r	-	8	-		
Turn-off Delay Time	$t_{d(OFF)}$	-	25	-		
Turn-off Fall Time	t_f	-	54	-		

Gate Charge Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Total Gate Charge	Q_g	-	19	-	nC	$V_{GS}=6V, V_{DS}=40V, I_D=20A$
Gate-Source Charge	Q_{gs}	-	8.9	-		$V_{GS}=10V, V_{DS}=40V,$ $I_D=20A$
Gate-Drain Charge	Q_{gd}	-	7.4	-		

Source Drain Diode Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Diode Forward Voltage	$V_{SD}^{(4)}$	-	0.8	1.1	V	$I_{SD}=10A, V_{GS}=0V$
Reverse Recovery Time	t_{rr}	-	25	-	nS	$I_F=10A, V_R=40V$ & $di_F/dt=100A/\mu s$
Reverse Recovery Charge	Q_{rr}	-	17	-	nC	

- ⁽⁴⁾ Pulse test (pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$).
- ⁽⁵⁾ Guaranteed by design, not subject to production test

Electrical characteristics diagrams

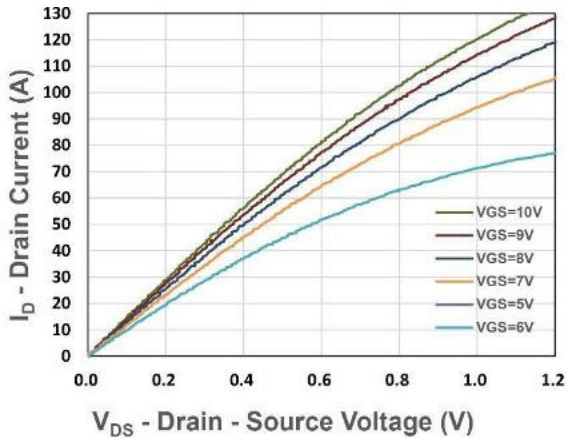


Figure 1. Output Characteristics

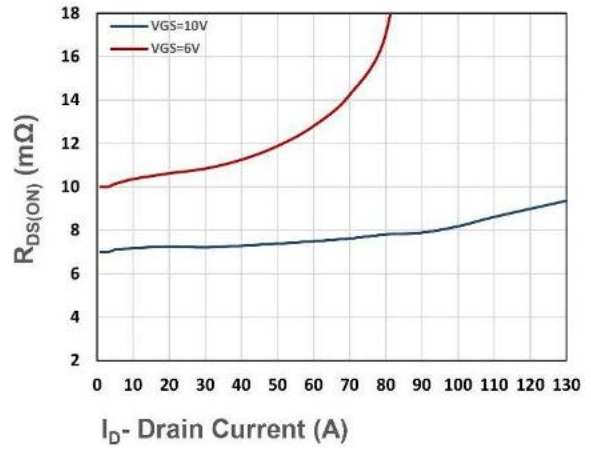


Figure 2. On-Resistance vs. I_D

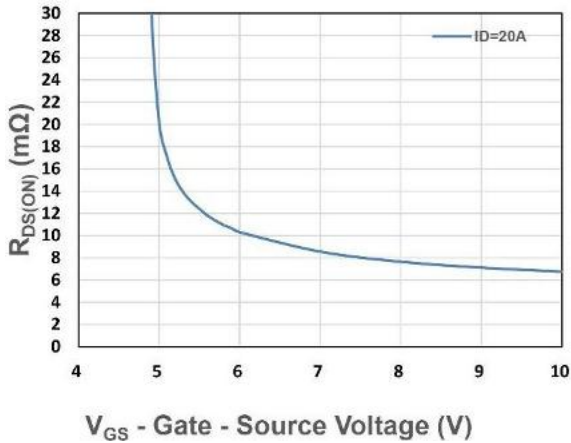


Figure 3. On-Resistance vs. V_{GS}

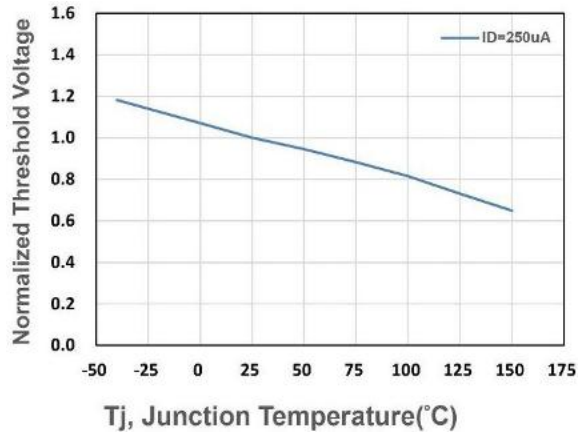


Figure 4. Gate Threshold Voltage

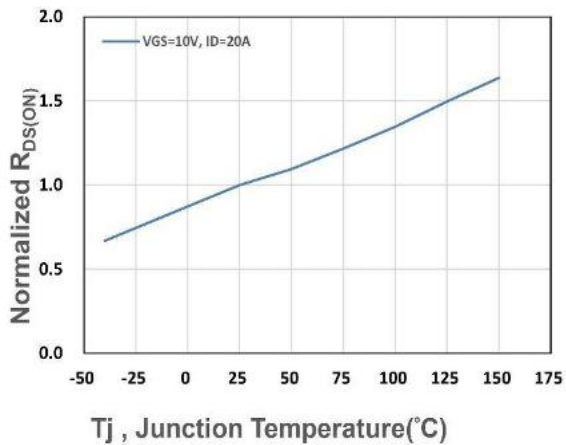


Figure 5. Drain-Source On Resistance

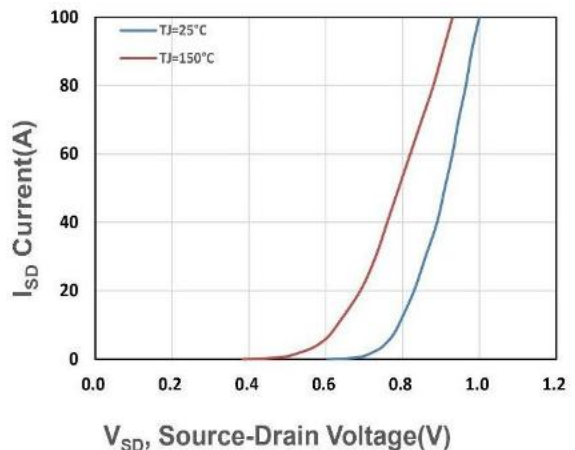
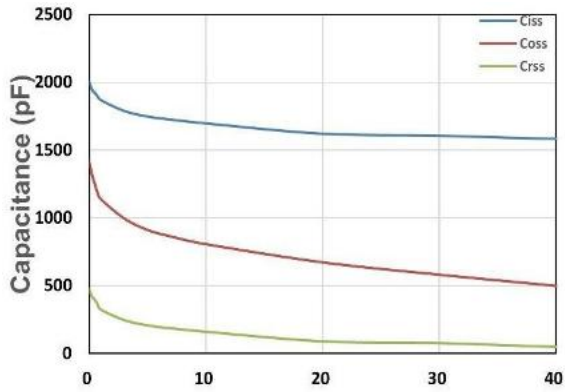
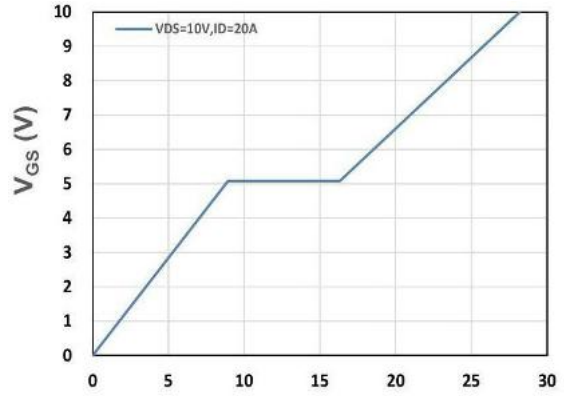


Figure 6. Source-Drain Diode Forward



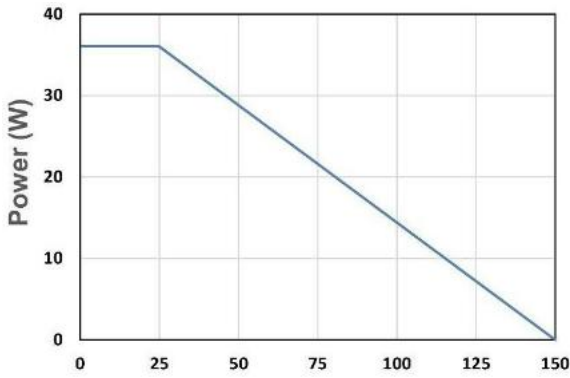
V_{DS} - Drain - Source Voltage (V)

Figure 7. Capacitance



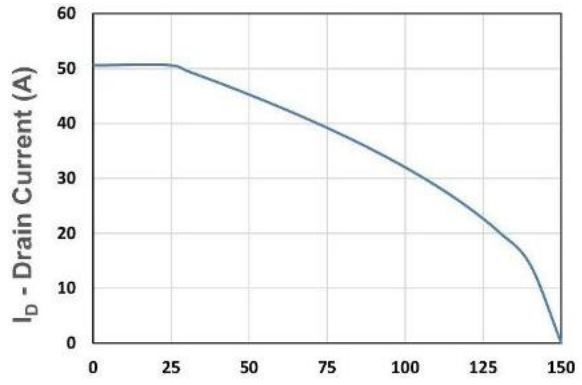
Q_g , Total Gate Charge (nC)

Figure 8. Gate Charge Characteristics



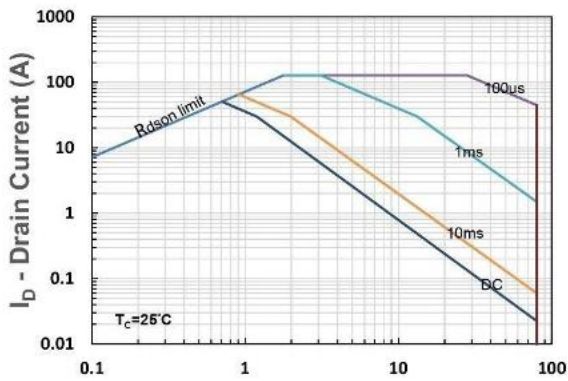
T_c - Case Temperature (°C)

Figure 9. Power Dissipation



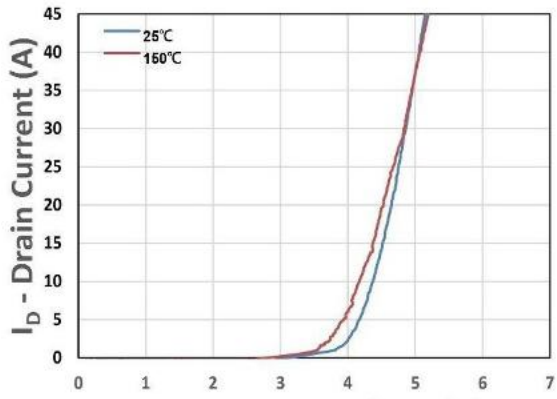
T_c - Case Temperature (°C)

Figure 10. Drain Current



V_{DS} - Drain-Source Voltage (V)

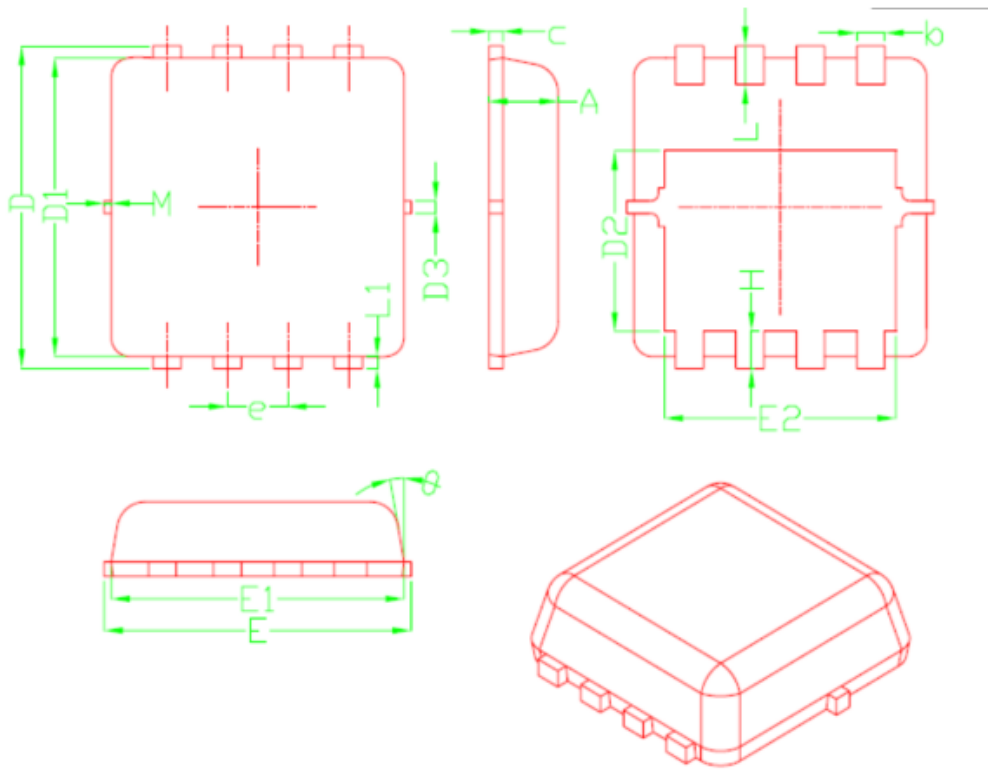
Figure 11. Safe Operating Area



V_{GS} - Gate - Source Voltage (V)

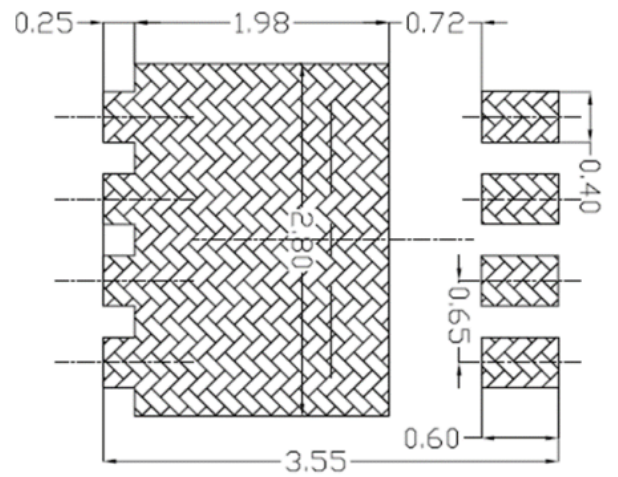
Figure 12. $R_{\theta JC}$ Transient Thermal Impedance

Package Information (PDFN3.3*3.3)



Outline Dimensions in mm

Unit:mm	Min	Typ	Max
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.15	0.25
D	3.25	3.35	3.45
D1	3.00	3.10	3.20
D2	1.78	1.88	1.98
D3	-	0.13	-
E	3.20	3.30	3.40
E1	3.00	3.15	3.20
E2	2.39	2.49	2.59
e	0.65 BSC		
H	0.30	0.39	0.50
L	0.30	0.40	0.50
L1	-	0.13	-
θ	-	10°	12°
M	-	-	0.15



Suggested Pad Layout (Unit:mm)

Disclaimer

The information provided in this datasheet is believed to be accurate and reliable. Errors or omissions are expected. indiaVP Semiconductor Pvt. Ltd. reserves the right to make changes to the product specifications without prior notice. Users should verify the suitability of the product for their specific applications. Please visit our website for the latest datasheet.

Contact Information

indiaVP Semiconductor Pvt. Ltd.

Email: sales@ivpsemi.com

Website: www.ivpsemi.com