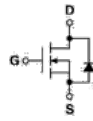


**LFPAK56**

**Symbol**


Parameter	Value	Unit
$V_{DS}$	45	V
$R_{DS(ON)-Max}$	0.8	mΩ
$I_D$	323	A

### Key Features

- Fast switching speed
- Reliable and Rugged
- ROHS Compliant & Halogen-Free
- 100% Avalanche / Rg Tested

### Applications

- DC-to-DC converters
- Switch Mode Power Supply

## Ordering Information

Ordering part Number	Marking code	Package	Form
VPLMDF7117	7117	LFPAK56	Tape & Reel

## Absolute Maximum Ratings (T<sub>j</sub> = 25°C, unless otherwise specified)

Parameter	Symbol	N-Channel	Unit
Drain-Source Voltage	$V_{DS}$	45	V
Gate-Source Voltage	$V_{GS}$	±20	V
Maximum Junction Temperature	$T_J$	175	°C
Storage Temperature Range	$T_{STG}$	-55 to 175	°C
Diode Continuous Forward Current	$I_S$	108	A
Pulse Drain Current Tested	$I_{DM}$	807 <sup>(1)</sup>	A
Continuous Drain Current	$I_D$	$T_C=25^\circ C$	323
		$T_C=100^\circ C$	228
Maximum Power Dissipation	$P_D$	$T_C=25^\circ C$	166
		$T_C=100^\circ C$	83
Continuous Drain Current	$I_D$	$T_A=25^\circ C$	46
		$T_A=70^\circ C$	38
Maximum Power Dissipation	$P_D$	$T_A=25^\circ C$	3.3
		$T_A=70^\circ C$	2.3
Avalanche Current, Single pulse	$I_{AS}^{(2)}$	L=0.1mH	55
		L=0.5mH	30
Avalanche Energy, Single pulse	$E_{AS}^{(2)}$	L=0.1mH	151
		L=0.5mH	225

## Thermal Characteristics

Parameter	Symbol	Rating	Unit
Thermal Resistance-Junction to Case	$R_{\theta JC}$	0.9	°C/W
Thermal Resistance-Junction to Ambient	$R_{\theta JA}^{(3)}$	45	°C/W

- <sup>(1)</sup> Max. current is limited by maximum junction temperature.
- <sup>(2)</sup> UIS tested and pulse width are limited by maximum junction temperature 175°C
- <sup>(3)</sup> Surface Mounted on 1in<sup>2</sup> FR-4 board with 1oz.

**Electrical Characteristics** (T<sub>j</sub> = 25°C, unless otherwise specified)

**Static Characteristics**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	45	-	-	V	V <sub>GS</sub> =0V, I <sub>DS</sub> =250uA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	-	-	1	uA	V <sub>DS</sub> =36V, V <sub>GS</sub> =0V
Gate Threshold Voltage	V <sub>GS(th)</sub>	2.4	2.9	3.5	V	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>DS</sub> =250uA
Gate Leakage Current	I <sub>GSS</sub>	-	-	±100	nA	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V
Drain-Source On-state Resistance	R <sub>DS(ON)</sub> <sup>(4)</sup>	-	0.66	0.8	mΩ	V <sub>GS</sub> =10V, I <sub>DS</sub> =50A
Forward Transconductance	g <sub>fs</sub>	-	44	-	S	V <sub>DS</sub> =5V, I <sub>DS</sub> =10A

**Dynamic Characteristics<sup>(5)</sup>**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Gate Resistance	R <sub>G</sub>	-	0.6	-	Ω	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, Freq.=1MHz
Input Capacitance	C <sub>iss</sub>	-	6281	-	pF	V <sub>GS</sub> =0V, V <sub>DS</sub> =20V, Freq.=1MHz
Output Capacitance	C <sub>oss</sub>	-	2159	-		
Reverse Transfer Capacitance	C <sub>rss</sub>	-	103	-		
Turn-on Delay Time	t <sub>d(ON)</sub>	-	20	-	nS	V <sub>GS</sub> =10V, V <sub>DS</sub> =25V, I <sub>D</sub> =1A, R <sub>GEN</sub> =1Ω
Turn-on Rise Time	t <sub>r</sub>	-	11	-		
Turn-off Delay Time	t <sub>d(OFF)</sub>	-	48	-		
Turn-off Fall Time	t <sub>f</sub>	-	100	-		

**Gate Charge Characteristics**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Total Gate Charge	Q <sub>g</sub>	-	83	-	nC	V <sub>GS</sub> =10V, V <sub>DS</sub> =25V, I <sub>D</sub> =20A
Gate-Source Charge	Q <sub>gs</sub>	-	25	-		
Gate-Drain Charge	Q <sub>gd</sub>	-	12	-		

**Source Drain Diode Characteristics**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Diode Forward Voltage	V <sub>SD</sub> <sup>(4)</sup>	-	0.74	-	V	I <sub>SD</sub> =10A, V <sub>GS</sub> =0V
Reverse Recovery Time	t <sub>rr</sub>	-	68	-	nS	I <sub>F</sub> =10A, V <sub>R</sub> =25V & dI <sub>F</sub> /dt=100A/μs
Reverse Recovery Charge	Q <sub>rr</sub>	-	98	-	nC	

- <sup>(4)</sup> Pulse test (pulse width ≤ 300us, duty cycle ≤ 2%).
- <sup>(5)</sup> Guaranteed by design, not subject to production testing.

## Electrical Characteristics Diagrams

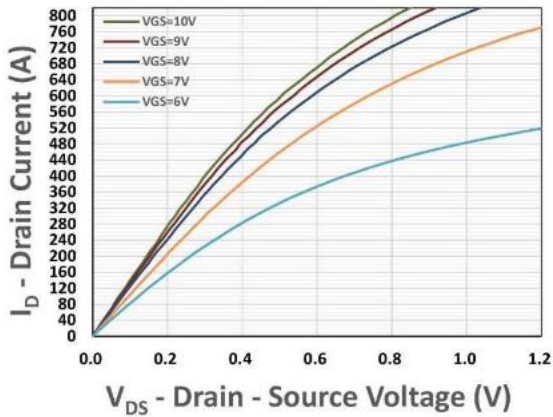


Figure 1. Output Characteristics

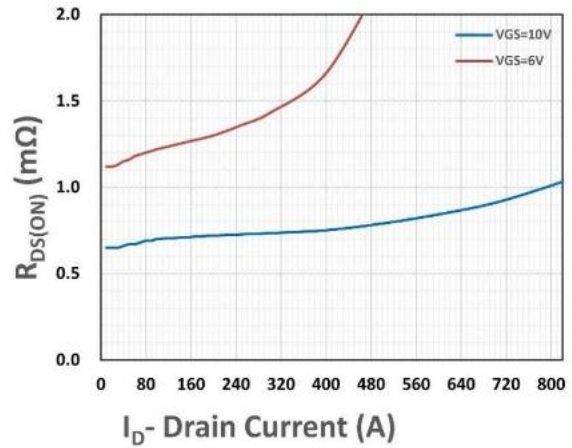


Figure 2. On-Resistance vs. ID

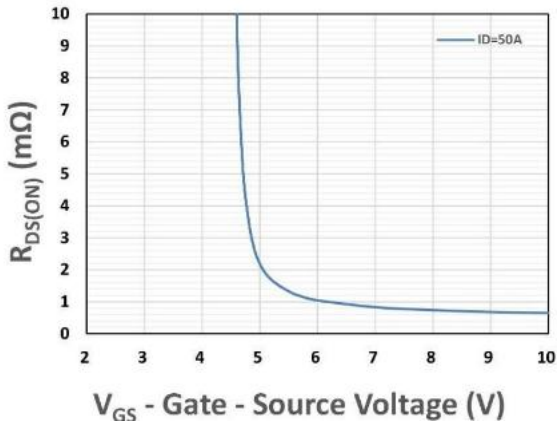


Figure 3. On-Resistance vs. VGS

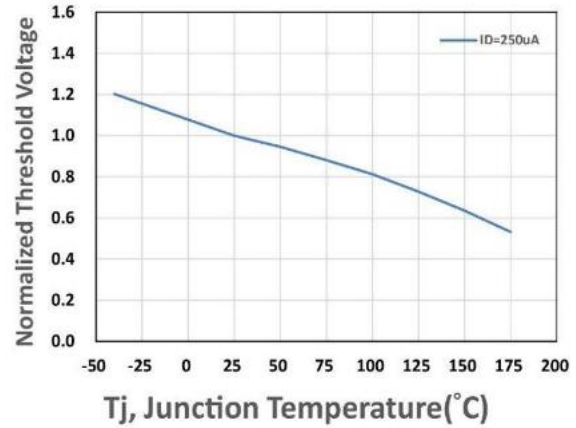


Figure 4. Gate Threshold Voltage

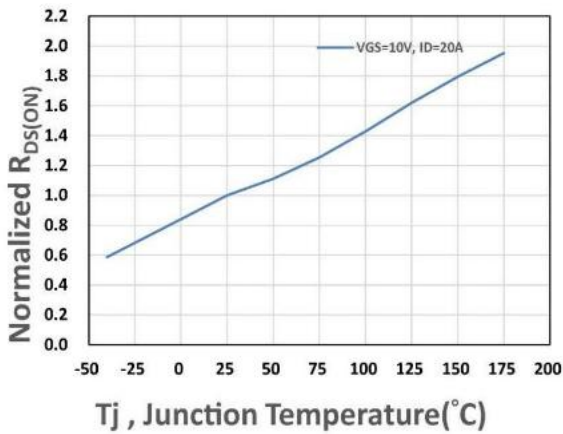


Figure 5. Drain-Source On Resistance

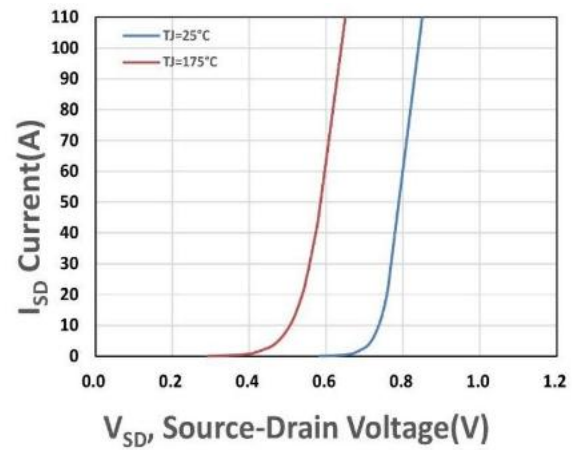


Figure 6. Source-Drain Diode Forward

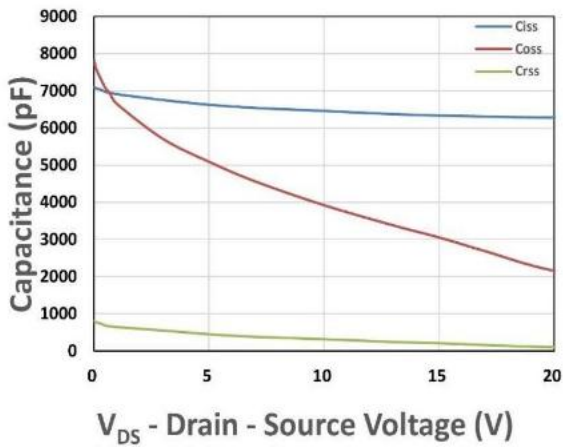


Figure 7. Capacitance

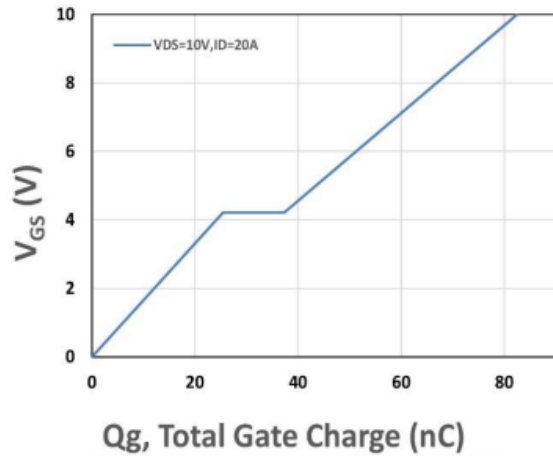


Figure 8. Gate Charge Characteristics

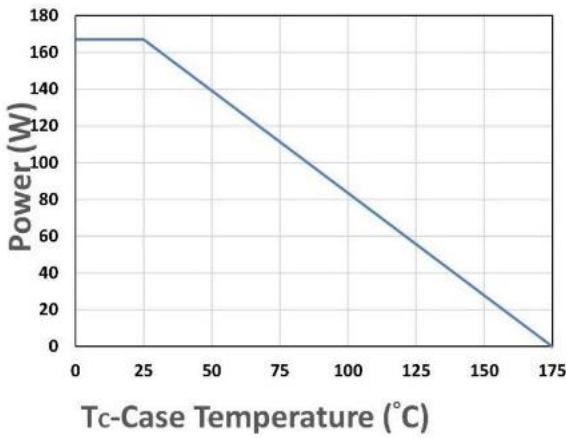


Figure 9. Power Dissipation

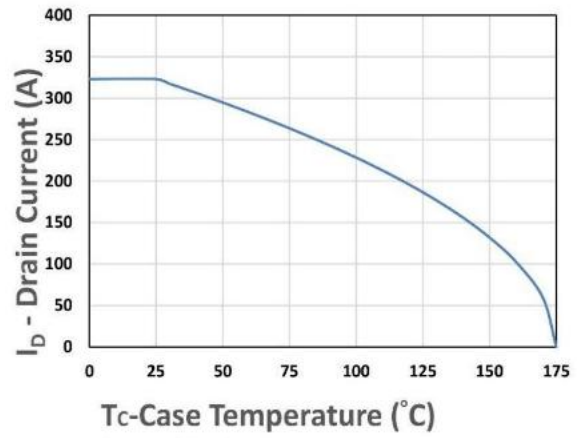


Figure 10. Drain Current

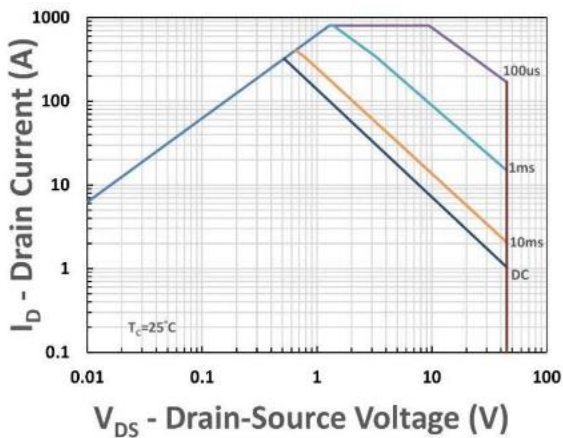


Figure 11. Safe Operating Area

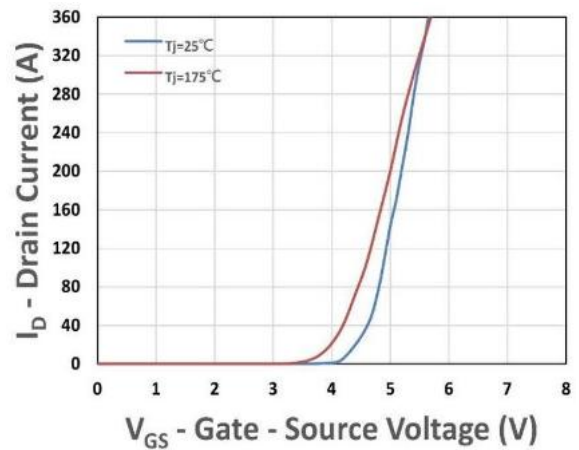


Figure 12. Transfer Characteristics

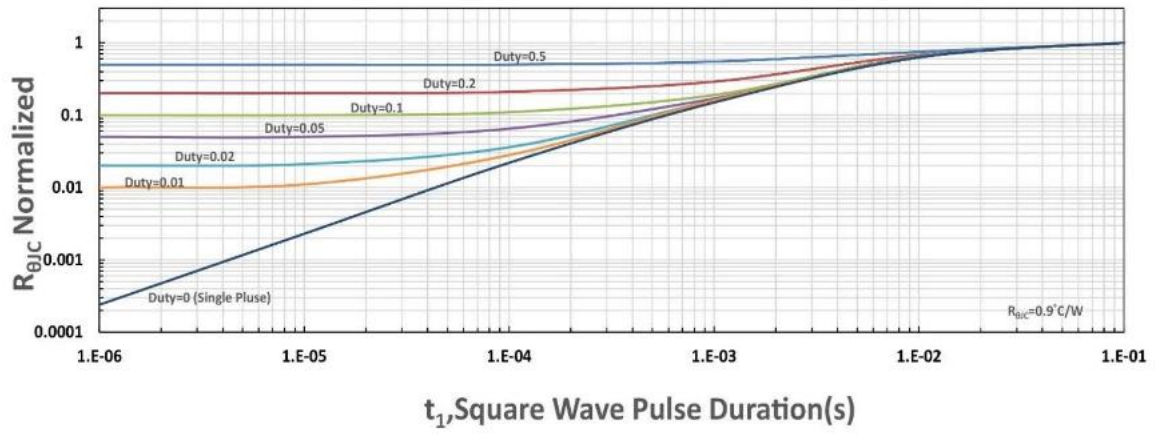
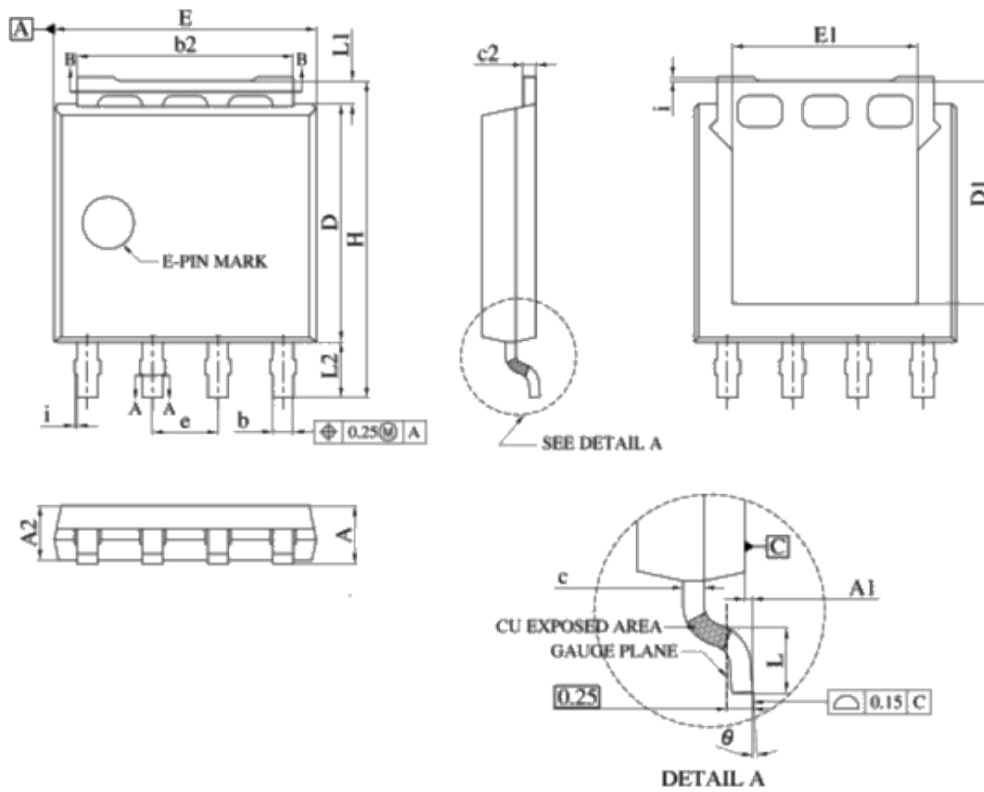


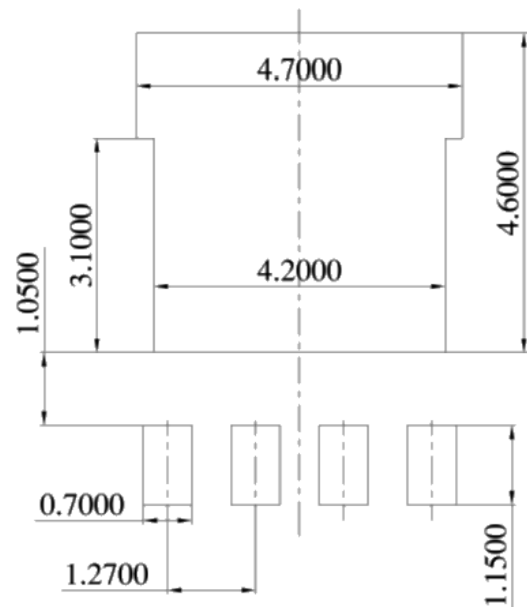
Figure 13.  $R_{\theta JC}$  Transient Thermal Impedance

Package Information (LFPAK56)



Outline dimensions in mm

Unit:mm	Min	Typ	Max
A	1.000	-	1.300
A1	0.000	0.075	0.150
A2	0.980	1.050	1.120
b	0.350	0.420	0.500
b2	4.020	4.230	4.410
c	0.190	0.220	0.250
c2	0.240	0.270	0.300
D	4.450	-	4.700
D1	-	-	4.450
E	4.950	-	5.300
E1	3.500	-	3.700
e	1.27 BSC		
H	5.950	-	6.250
i	-	-	0.250
L	0.400	-	0.850
L1	0.270	-	0.570
L2	0.800	-	1.300
$\theta$	0°	-	8°



Suggested Pad Layout (Unit:mm)

**Disclaimer**

The information provided in this datasheet is believed to be accurate and reliable. Errors or omissions are expected. indiaVP Semiconductor Pvt. Ltd. reserves the right to make changes to the product specifications without prior notice. Users should verify the suitability of the product for their specific applications. Please visit our website for the latest datasheet.

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