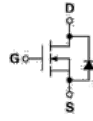


**LFPAK56**

**Symbol**


Parameter	Value	Unit
$V_{DS}$	25	V
$R_{DS(ON)-Max}$	0.7	m $\Omega$
$I_D$	321	A

**Key Features**

- Reliable and Rugged
- ROHS Compliant & Halogen-Free
- 100% UIS and Rg Tested

**Applications**

- Power Load Switch
- Oring FETs

**Ordering Information**

Ordering part Number	Marking code	Package	Form
VPLMDF7110	7110	LFPAK56	Tape & Reel

**Absolute Maximum Ratings** ( $T_j = 25^\circ\text{C}$ , unless otherwise specified)

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	$V_{DS}$	25	V
Gate-Source Voltage	$V_{GS}$	$\pm 16$	V
Maximum Junction Temperature	$T_J$	175	$^\circ\text{C}$
Storage Temperature Range	$T_{STG}$	-55 to 175	$^\circ\text{C}$
Diode Continuous Forward Current	$I_S$	57	A
Pulse Drain Current Tested	$I_{DM}$	803 <sup>(1)</sup>	A
Continuous Drain Current	$I_D$	$T_C=25^\circ\text{C}$	321
		$T_C=100^\circ\text{C}$	227
Maximum Power Dissipation	$P_D$	$T_C=25^\circ\text{C}$	125
		$T_C=100^\circ\text{C}$	62.5
Continuous Drain Current	$I_D^{(2)}$	$T_A=25^\circ\text{C}$	52.5
		$T_A=70^\circ\text{C}$	44
Maximum Power Dissipation	$P_D^{(2)}$	$T_A=25^\circ\text{C}$	3.3
		$T_A=70^\circ\text{C}$	2.3
Avalanche Current, Single pulse	$I_{AS}^{(3)}$	L=0.1mH	63
		L=0.5mH	40
Avalanche Energy, Single pulse	$E_{AS}^{(3)}$	L=0.1mH	198
		L=0.5mH	400

**Thermal Characteristics**

Parameter	Symbol	Rating	Unit
Thermal Resistance-Junction to Case	$R_{\theta JC}$	1.2	$^\circ\text{C/W}$
Thermal Resistance-Junction to Ambient	$R_{\theta JA}^{(2)}$	45	$^\circ\text{C/W}$

- <sup>(1)</sup> Max. current is limited by junction temperature.
- <sup>(2)</sup> Surface Mounted on 1in<sup>2</sup> FR-4 board with 1oz.
- <sup>(3)</sup> UIS tested and pulse width are limited by maximum junction temperature 175 $^\circ\text{C}$

**Electrical Characteristics** ( $T_j = 25^\circ\text{C}$ , unless otherwise specified)

**Static Characteristics**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	25	-	-	V	$V_{GS}=0V, I_{DS}=250\mu A$
Zero Gate Voltage Drain Current	$I_{DSS}$	-	-	1	$\mu A$	$V_{DS}=20V, V_{GS}=0V$
Gate Threshold Voltage	$V_{GS(th)}$	1	1.5	2	V	$V_{DS}=V_{GS}, I_{DS}=250\mu A$
Gate Leakage Current	$I_{GSS}$	-	-	$\pm 100$	nA	$V_{GS}=\pm 16V, V_{DS}=0V$
Drain-Source On-state Resistance	$R_{DS(ON)}^{(4)}$	-	0.50	0.7	m $\Omega$	$V_{GS}=10V, I_{DS}=50A$
		-	0.75	1.0		$V_{GS}=4.5V, I_{DS}=25A$
Forward Transconductance	$g_{fs}$	-	66	-	S	$V_{DS}=5V, I_{DS}=10A$

**Dynamic Characteristics<sup>(5)</sup>**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Gate Resistance	$R_G$	-	3	-	$\Omega$	$V_{GS}=0V, V_{DS}=0V,$ Freq.=1MHz
Input Capacitance	$C_{iss}$	-	6931	-	pF	$V_{GS}=0V, V_{DS}=12.5V,$ Freq.=1MHz
Output Capacitance	$C_{oss}$	-	1204	-		
Reverse Transfer Capacitance	$C_{rss}$	-	851	-		
Turn-on Delay Time	$t_{d(ON)}$	-	15	-	nS	$V_{GS}=10V, V_{DS}=12.5V,$ $I_D=1A, R_{GEN}=1\Omega$
Turn-on Rise Time	$t_r$	-	14	-		
Turn-off Delay Time	$t_{d(OFF)}$	-	141	-		
Turn-off Fall Time	$t_f$	-	39	-		

**Gate Charge Characteristics**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Total Gate Charge	$Q_g$	-	80	-	nC	$V_{GS}=4.5V, V_{DS}=12.5V,$ $I_D=50A$
		-	178	-		$V_{GS}=10V, V_{DS}=12.5V,$ $I_D=50A$
Gate-Source Charge	$Q_{gs}$	-	25	-		
Gate-Drain Charge	$Q_{gd}$	-	18	-		

**Source Drain Diode Characteristics**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Diode Forward Voltage	$V_{SD}^{(4)}$	-	0.7	1.1	V	$I_{SD}=25A, V_{GS}=0V$
Reverse Recovery Time	$t_{rr}$	-	38	-	nS	$I_F=25A, V_R=15V$ & $di_F/dt=100A/\mu s$
Reverse Recovery Charge	$Q_{rr}$	-	41	-	nC	

- <sup>(4)</sup> Pulse test (pulse width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$ ).
- <sup>(5)</sup> Guaranteed by design, not subject to production test

## Electrical Characteristics Diagrams

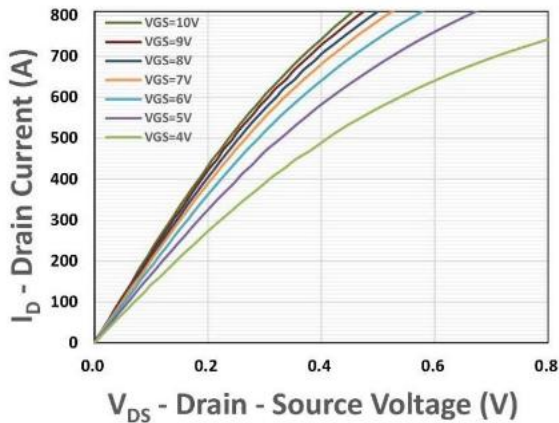


Figure 1. Output Characteristics

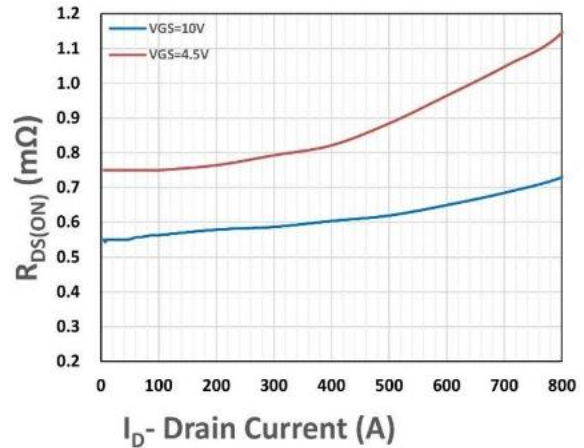


Figure 2. On-Resistance vs.  $I_D$

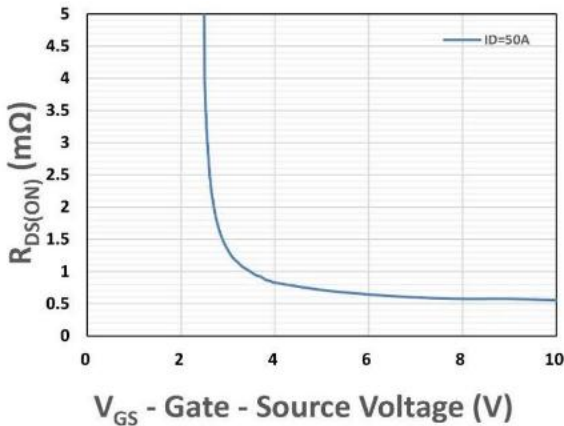


Figure 3. On-Resistance vs.  $V_{GS}$

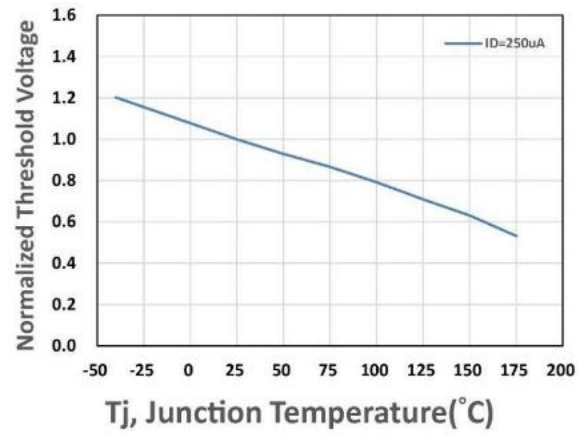


Figure 4. Gate Threshold Voltage

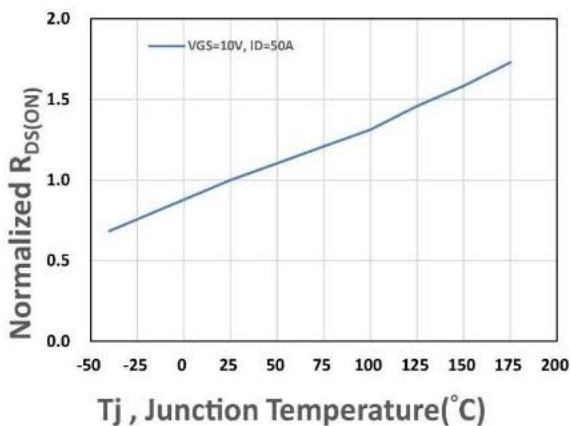


Figure 5. Drain-Source On Resistance

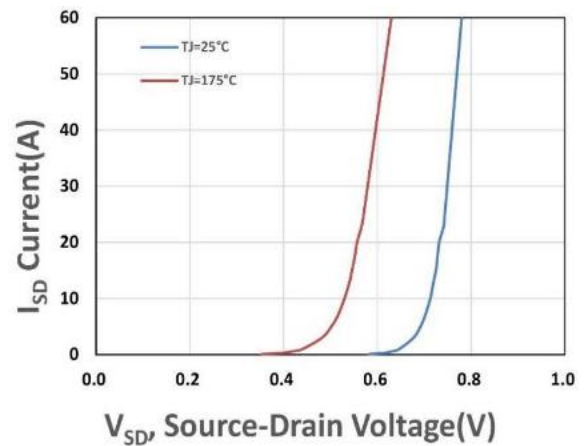


Figure 6. Source-Drain Diode Forward

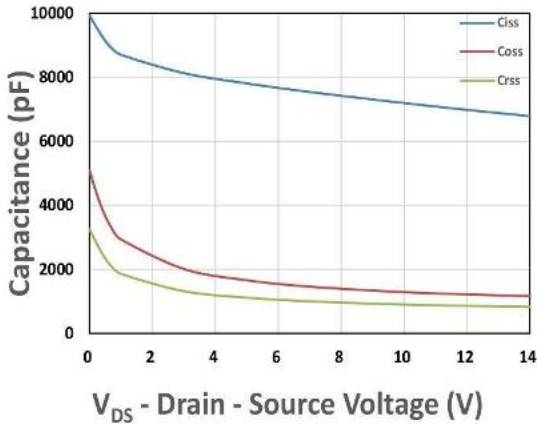


Figure 7. Capacitance

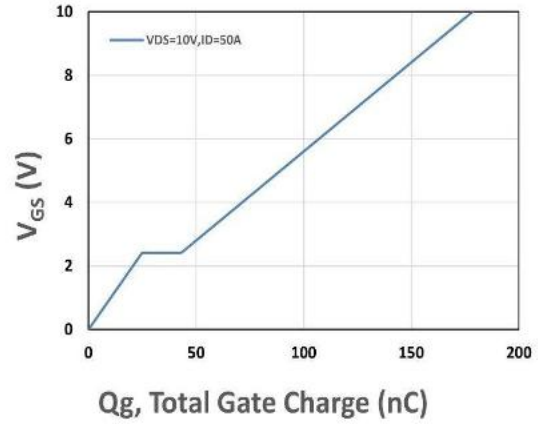


Figure 8. Gate Charge Characteristics

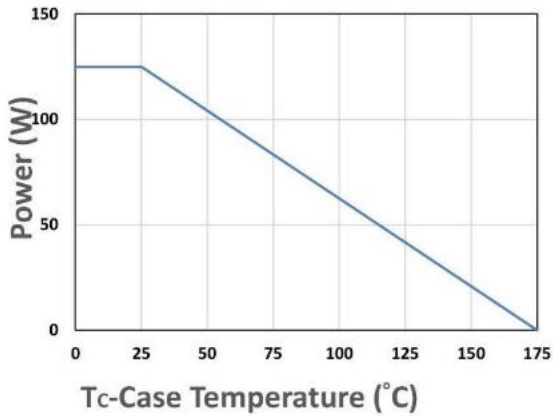


Figure 9. Power Dissipation

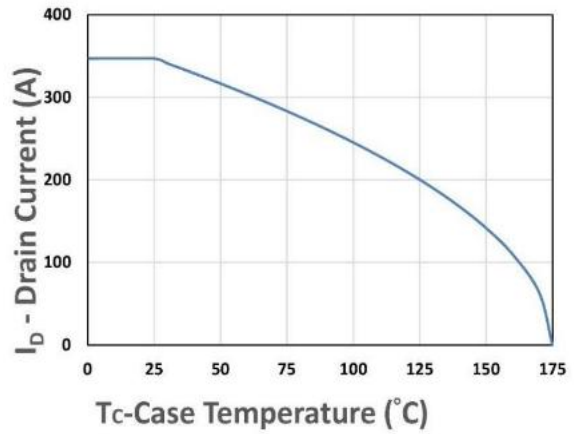


Figure 10. Drain Current

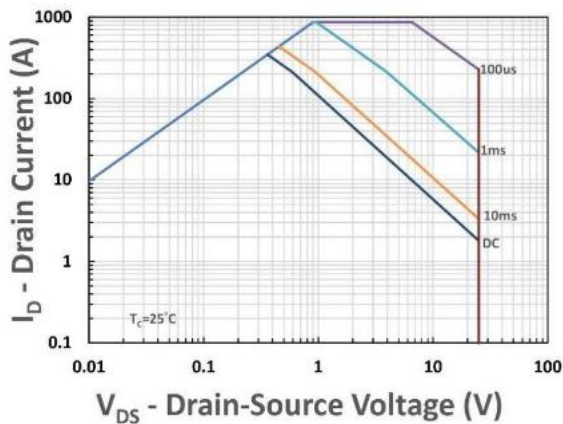


Figure 11. Safe Operating Area

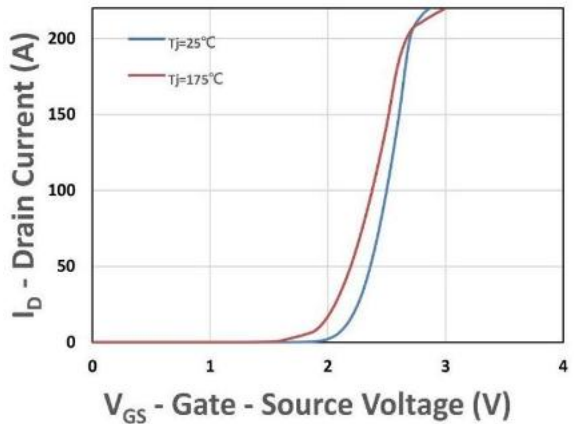


Figure 12. Transfer Characteristics

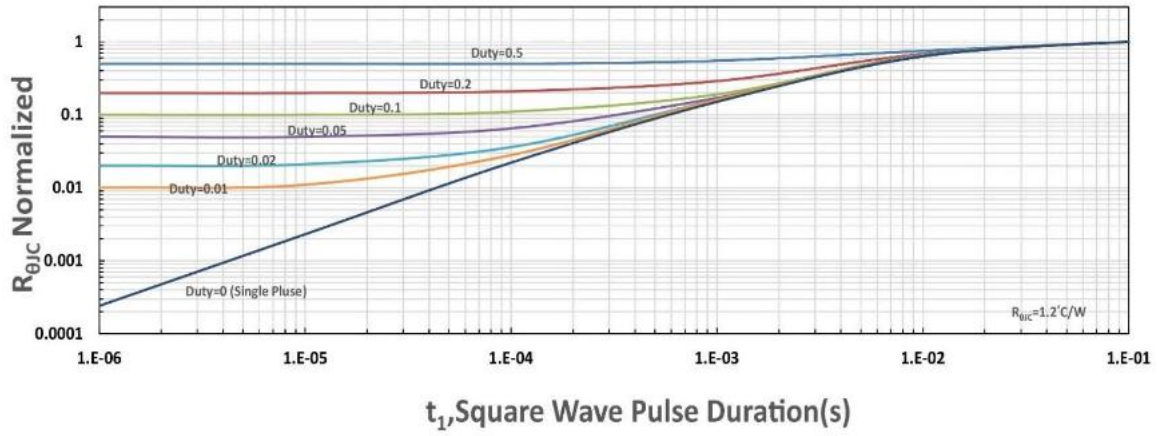
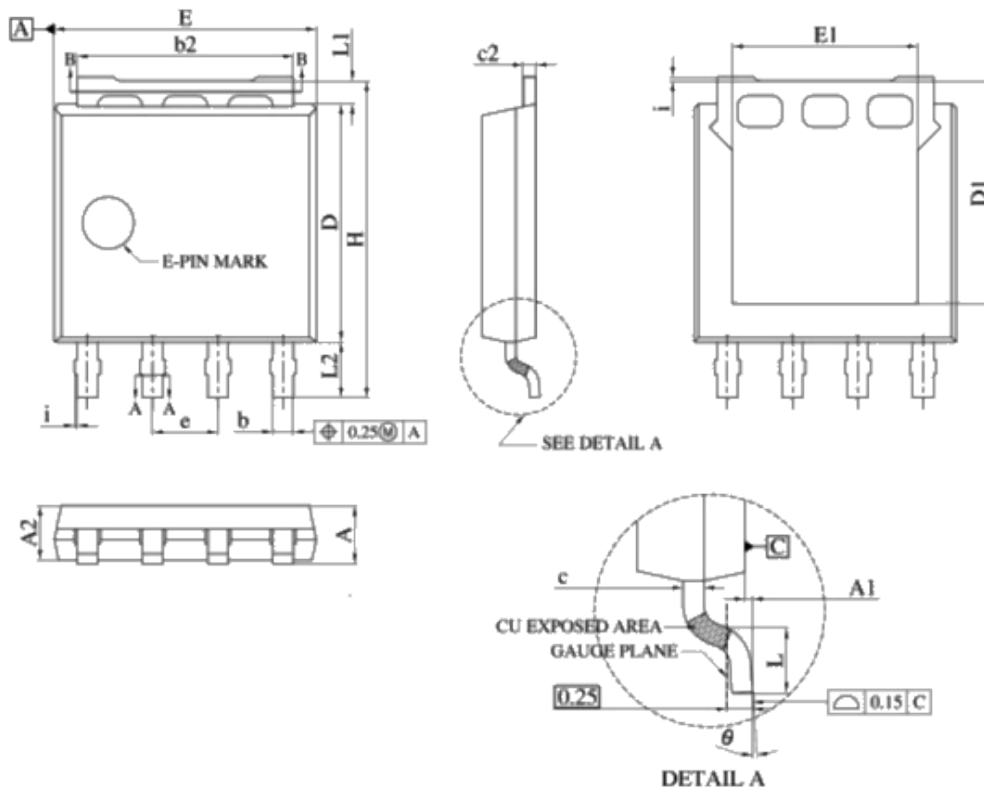


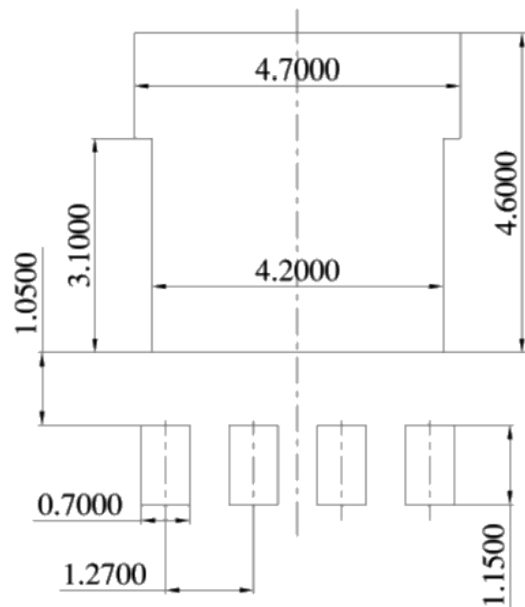
Figure 13.  $R_{\theta JC}$  Transient Thermal Impedance

Package Information (LFPAK56)



Outline dimensions in mm

Unit:mm	Min	Typ	Max
A	1.000	-	1.300
A1	0.000	0.075	0.150
A2	0.980	1.050	1.120
b	0.350	0.420	0.500
b2	4.020	4.230	4.410
c	0.190	0.220	0.250
c2	0.240	0.270	0.300
D	4.450	-	4.700
D1	-	-	4.450
E	4.950	-	5.300
E1	3.500	-	3.700
e	1.27 BSC		
H	5.950	-	6.250
i	-	-	0.250
L	0.400	-	0.850
L1	0.270	-	0.570
L2	0.800	-	1.300
θ	0°	-	8°



Suggested Pad Layout (Unit:mm)

**Disclaimer**

The information provided in this datasheet is believed to be accurate and reliable. Errors or omissions are expected. indiaVP Semiconductor Pvt. Ltd. reserves the right to make changes to the product specifications without prior notice. Users should verify the suitability of the product for their specific applications. Please visit our website for the latest datasheet.

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